4.20.4– 184 PIN, PC1800/2100 DDR SDRAM REGISTERED DIMM DESIGN SPECIFICATION

PC1800/2100 DDR SDRAM Registered DIMM

Design Specification

Revision 1.1

Contents

Product Description

This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100, 64/72-bit wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs).These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC1600/PC2100 refers to the JEDEC standard DIMM naming convention in which PC1600 indicates a 184-pin DIMM running at 100 MHz clock speed and offering 1600MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC1600/PC2100 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 184-pin Registered DDR SDRAM DIMM product (refer to JEDEC Standards Manual 21-C, at http://www.jedec.org).

Product Family Attributes

DIMM organization	x72 ECC, x64
DIMM dimensions (nominal)	5.25” x 1.7” x .157”/.320”
Pin count	184
SDRAMs supported	64Mb, 128Mb, 256Mb, 512Mb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB, 2GB
Serial PD	Consistent with JC 42.5, Rev 0
Voltage options	2.5 volt (V_{DD}/V_{DDQ})
Interface	SSTL_2

Environmental Requirements

DDR SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature (ambient)	0 to +55	∝C	1
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	∝C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or abouve the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

Architecture

Pin Description

Pin Name	Description	Pin Name	Description
A0 - A13	SDRAM address bus	$\overline{CK}0$	SDRAM clock (negative line of differential pair)
BA0 - BA1	SDRAM bank select	SCL	IIC serial bus clock for EEPROM
DQ0 - DQ63	DIMM memory data bus	SDA	IIC serial bus data line for EEPROM
CB0 - CB7	DIMM ECC check bits	SA0 - SA2	IIC slave address select for EEPROM
$\overline{RAS}$	SDRAM row address strobe	V_{DD}	SDRAM positive power supply
$\overline{CAS}$	SDRAM column address strobe	V_{DDQ}	SDRAM I/O Driver positive power supply
$\overline{WE}$	SDRAM write strobe	V_{REF}	SDRAM I/O reference supply
$\overline{S}0$ - $\overline{S}3$	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)	V_{SS}	Power supply return (ground)
CKE0 - CKE1	SDRAM clock enable lines	V_{DDSPD}	Serial EEPROM positive power supply (Supports both 2.5 Volt and 3.3 Volt operation)
DQS0 - DQS8	SDRAM low data strobes	NC	Spare Pins (no connect)
DM(0-8)/DQS(9-17)	SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs)	$\overline{RESET}$	Reset pin (forces register inputs low)
V_{DDID}	VDD Identification Flag	$\overline{FETEN}$	External control pin for DIMMs with FET switches in DQ path
CK0	SDRAM clock (positive line of differential pair)		

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	SSTL	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL. (All DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.)
$\overline{CK0}$	SSTL	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0, CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$, S2, S3	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0,1	SSTL	—	Selects which SDRAM bank of four is activated.
A0-A9, A11 A10/AP, A12, A13	SSTL	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A11 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	SSTL	—	Data and Check Bit Input/Output pins
DM0-DM8	SSTL	Active High	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0-DQS8	SSTL	Negative and Positive Edge	Data strobe for input and output data.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports both 2.3 Volt and 3.3 Volt operation).
$\overline{RESET}$	LV-CMOS	Active Low	This signal is asynchronous and driven low to the register to guarantee that the register outputs are low.
$\overline{FETEN}$	SSTL	Active Low	This signal is reserved for future FET switch DIMMs that may use external control to enable/disable FET pass gates in the DIMM data path. When high, devices are ‘off’ and in a high impedance state. When low, they are in a low impedance state and data can be read from or written to memory.

184-Pin DDR SDRAM DIMM Pin Assignments

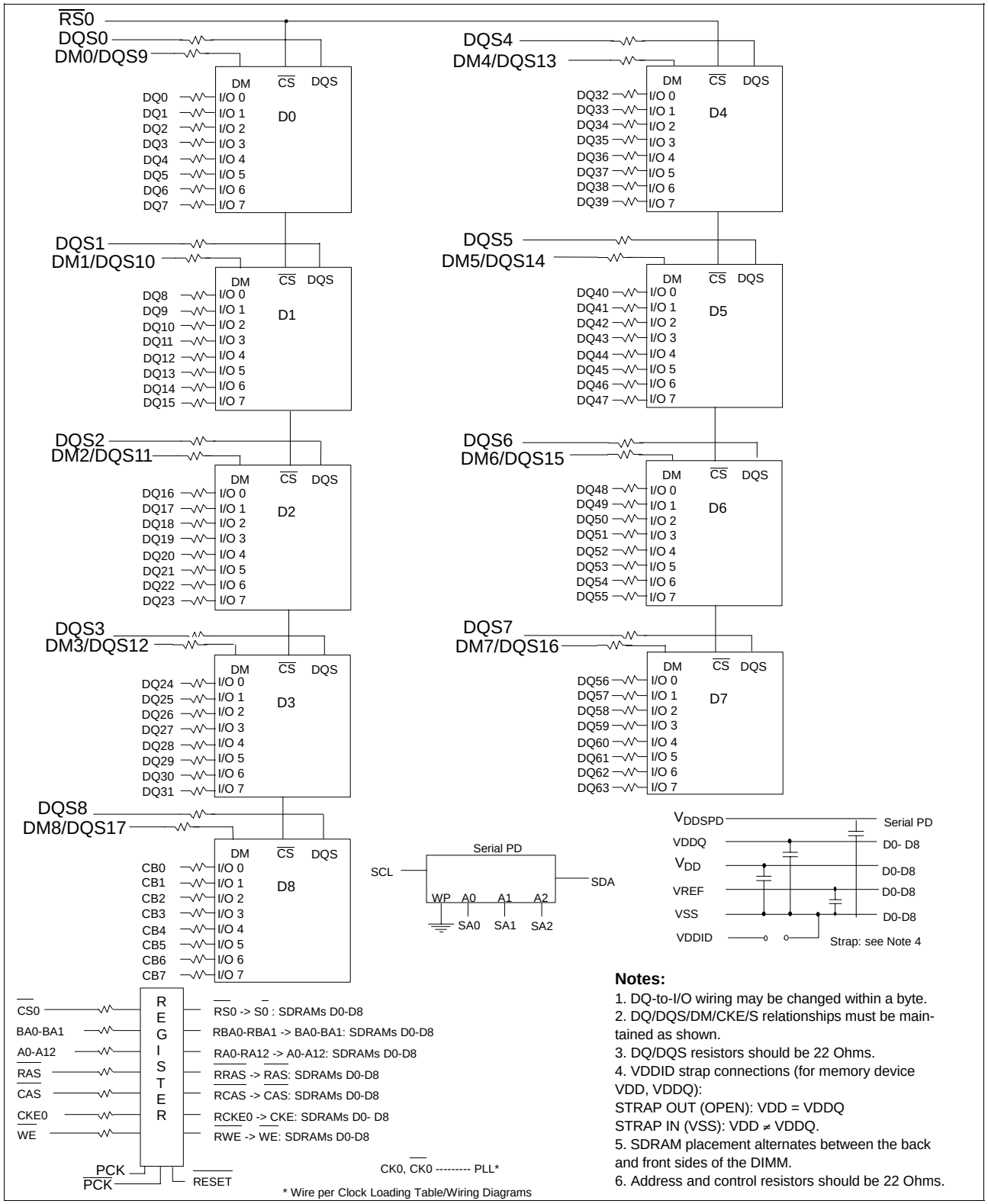
Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC
1	V_{REF}	V_{REF}	93	V_{SS}	V_{SS}	48	A0	A0	140	NC	DM8/DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10	A10
3	V_{SS}	V_{SS}	95	DQ5	DQ5	50	V_{SS}	V_{SS}	142	NC	CB6
4	DQ1	DQ1	96	V_{DDQ}	V_{DDQ}	51	NC	CB3	143	V_{DDQ}	V_{DDQ}
5	DQS0	DQS0	97	DM0/DQS9	DM0/DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	V_{DD}	V_{DD}	99	DQ7	DQ7	53	DQ32	DQ32	145	V_{SS}	V_{SS}
8	DQ3	DQ3	100	V_{SS}	V_{SS}	54	V_{DDQ}	V_{DDQ}	146	DQ36	DQ36
9	NC	NC	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	RESET	$\overline{\text{RESET}}$	102	NC	NC	56	DQS4	DQS4	148	V_{DD}	V_{DD}
11	V_{SS}	V_{SS}	103	$\overline{\text{FETN}}$, NC	$\overline{\text{FETN}}$, NC	57	DQ34	DQ34	149	DM4/DQS13	DM4/DQS13
12	DQ8	DQ8	104	V_{DDQ}	V_{DDQ}	58	V_{SS}	V_{SS}	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	V_{SS}	V_{SS}
15	V_{DDQ}	V_{DDQ}	107	DM1/DQS10	DM1/DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	DU (CK1)[1]	DU (CK1)[1]	108	V_{DD}	V_{DD}	62	V_{DDQ}	V_{DDQ}	154	RAS	RAS
17	DU ($\overline{\text{CK1}}$)[1]	DU ($\overline{\text{CK1}}$)[1]	109	DQ14	DQ14	63	WE	WE	155	DQ45	DQ45
18	V_{SS}	V_{SS}	110	DQ15	DQ15	64	DQ41	DQ41	156	V_{DDQ}	V_{DDQ}
19	DQ10	DQ10	111	CKE1	CKE1	65	CAS	CAS	157	$\overline{\text{S}}0$	$\overline{\text{S}}0$
20	DQ11	DQ11	112	V_{DDQ}	V_{DDQ}	66	V_{SS}	V_{SS}	158	$\overline{\text{S}}1$	$\overline{\text{S}}1$
21	CKE0	CKE0	113	NC(BA2)	NC(BA2)	67	DQS5	DQS5	159	DM5/DQS14	DM5/DQS14
22	V_{DDQ}	V_{DDQ}	114	DQ20	DQ20	68	DQ42	DQ42	160	V_{SS}	V_{SS}
23	DQ16	DQ16	115	A12, NC	A12, NC	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	V_{SS}	V_{SS}	70	V_{DD}	V_{DD}	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, $\overline{\text{S}}2$	NC, $\overline{\text{S}}2$	163	NC, $\overline{\text{S}}3$	NC, $\overline{\text{S}}3$
26	V_{SS}	V_{SS}	118	A11	A11	72	DQ48	DQ48	164	V_{DDQ}	V_{DDQ}
27	A9	A9	119	DM2/DQS11	DM2/DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	V_{DD}	V_{DD}	74	V_{SS}	V_{SS}	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	DU ($\overline{\text{CK2}}$)[1]	DU ($\overline{\text{CK2}}$)[1]	167	NC, A13	NC, A13
30	V_{DDQ}	V_{DDQ}	122	A8	A8	76	DU (CK2)[1]	DU (CK2)[1]	168	V_{DD}	V_{DD}
31	DQ19	DQ19	123	DQ23	DQ23	77	V_{DDQ}	V_{DDQ}	169	DM6/DQS15	DM6/DQS15
32	A5	A5	124	V_{SS}	V_{SS}	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	V_{SS}	V_{SS}	126	DQ28	DQ28	80	DQ51	DQ51	172	V_{DDQ}	V_{DDQ}
35	DQ25	DQ25	127	DQ29	DQ29	81	V_{SS}	V_{SS}	173	NC	NC
36	DQS3	DQS3	128	V_{DDQ}	V_{DDQ}	82	V_{DDID}	V_{DDID}	174	DQ60	DQ60
37	A4	A4	129	DM3/DQS12	DM3/DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	V_{DD}	V_{DD}	130	A3	A3	84	DQ57	DQ57	176	V_{SS}	V_{SS}
39	DQ26	DQ26	131	DQ30	DQ30	85	V_{DD}	V_{DD}	177	DM7/DQS16	DM7/DQS16
40	DQ27	DQ27	132	V_{SS}	V_{SS}	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	V_{SS}	V_{SS}	134	NC	CB4	88	DQ59	DQ59	180	V_{DDQ}	V_{DDQ}
43	A1	A1	135	NC	CB5	89	V_{SS}	V_{SS}	181	SA0	SA0
44	NC	CB0	136	V_{DDQ}	V_{DDQ}	90	DU	DU	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	V_{DD}	V_{DD}	138	CK0	CK0	92	SCL	SCL	184	V_{DDSPD}	V_{DDSPD}
47	NC	DQS8	139	V_{SS}	V_{SS}						

NC = No Connect; NU = Not Useable; DU = Do Not Use

1. These pins are used only with 256Mbit SDRAM devices. Systems supporting both unbuffered and registered DIMMs may may be connected to an active signal on the baseboard.

Block Diagram: Raw Card Version A

(x72 DIMM, populated as one physical bank of x8 DDR SDRAMs)

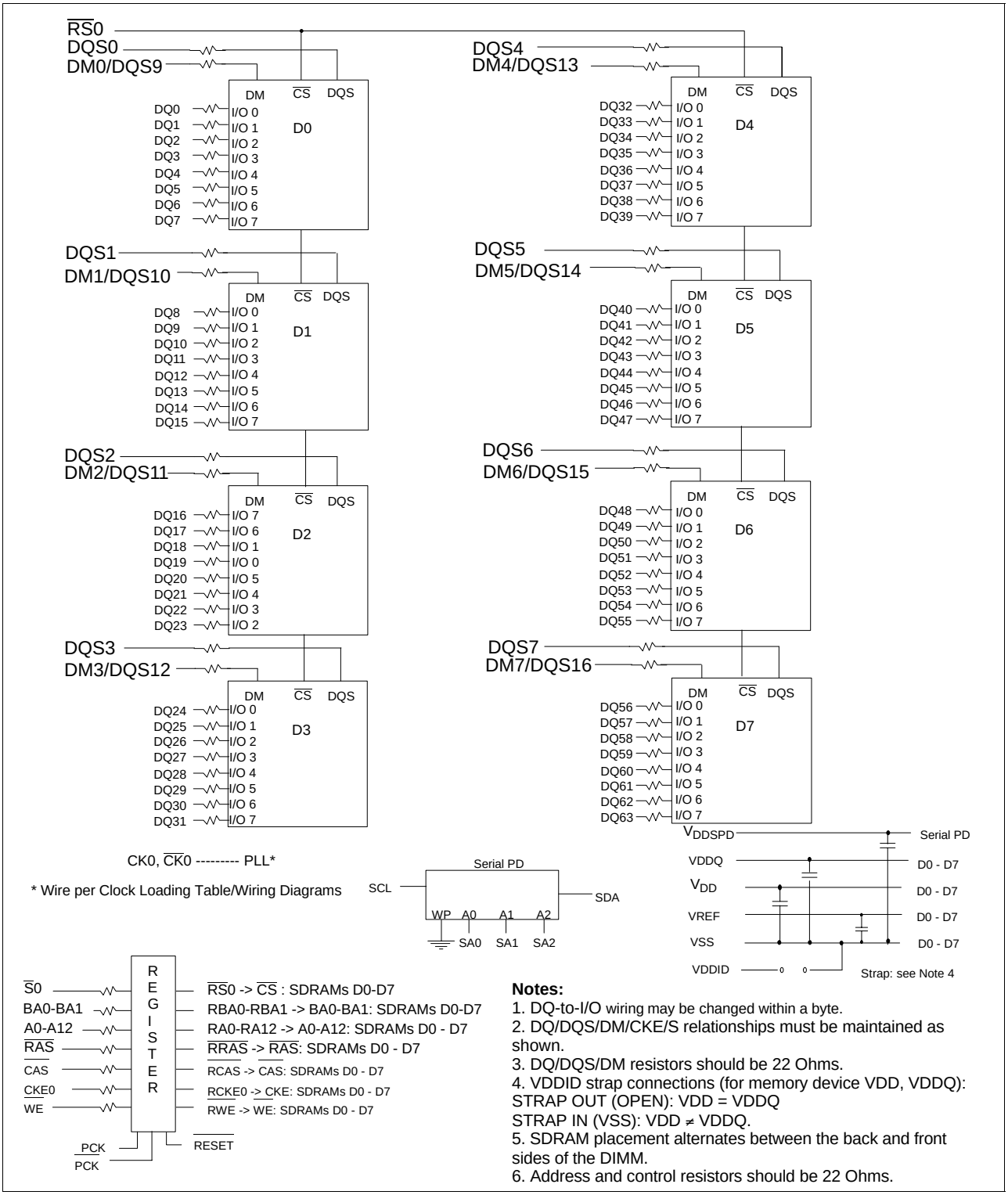


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

Block Diagram: Raw Card Version A

(x64 DIMM, populated as one physical bank of x8 DDR SDRAMs)

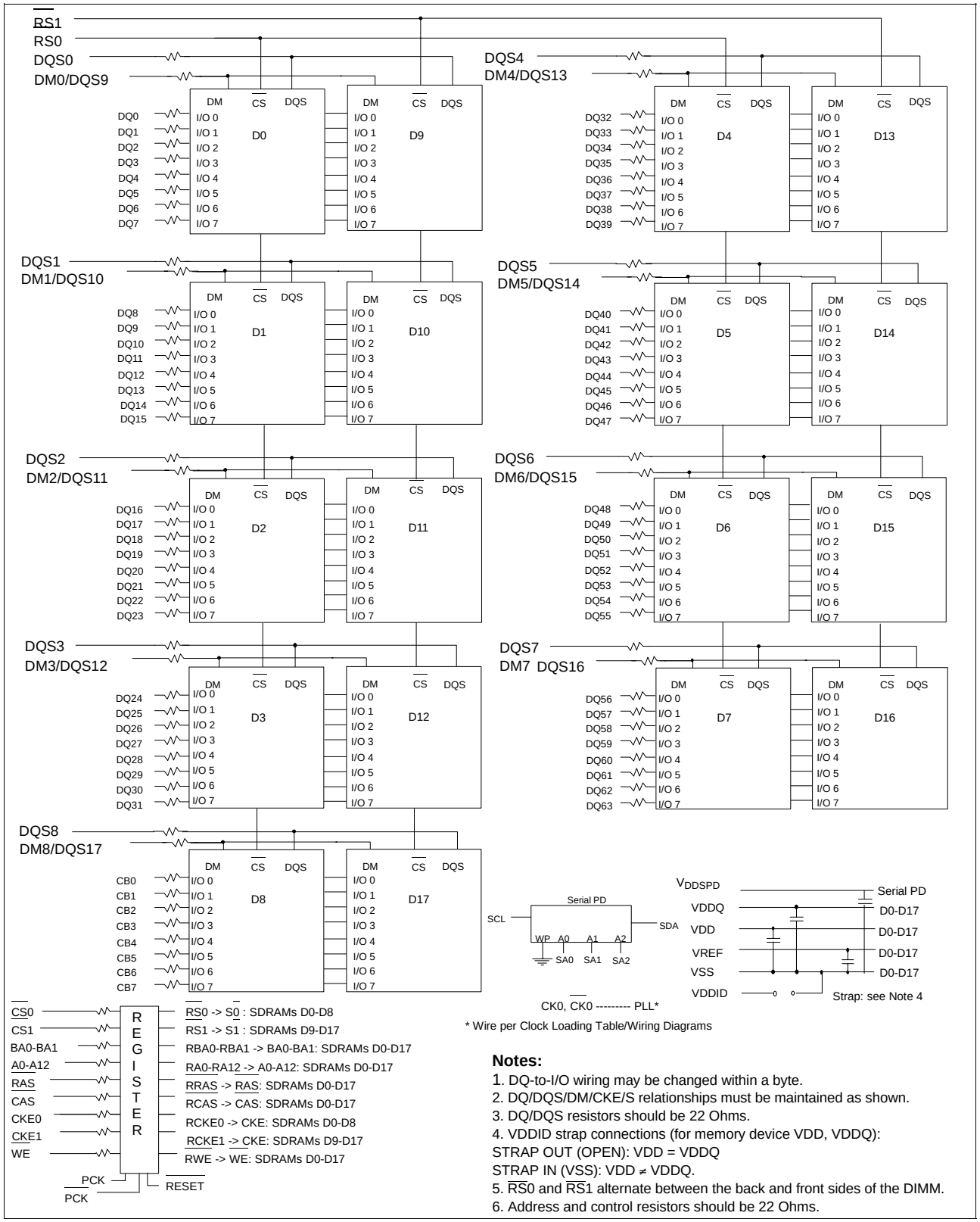


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

Block Diagram: Raw Card Version A

(x72 DIMM, populated as two physical banks of x8 DDR SDRAMs)

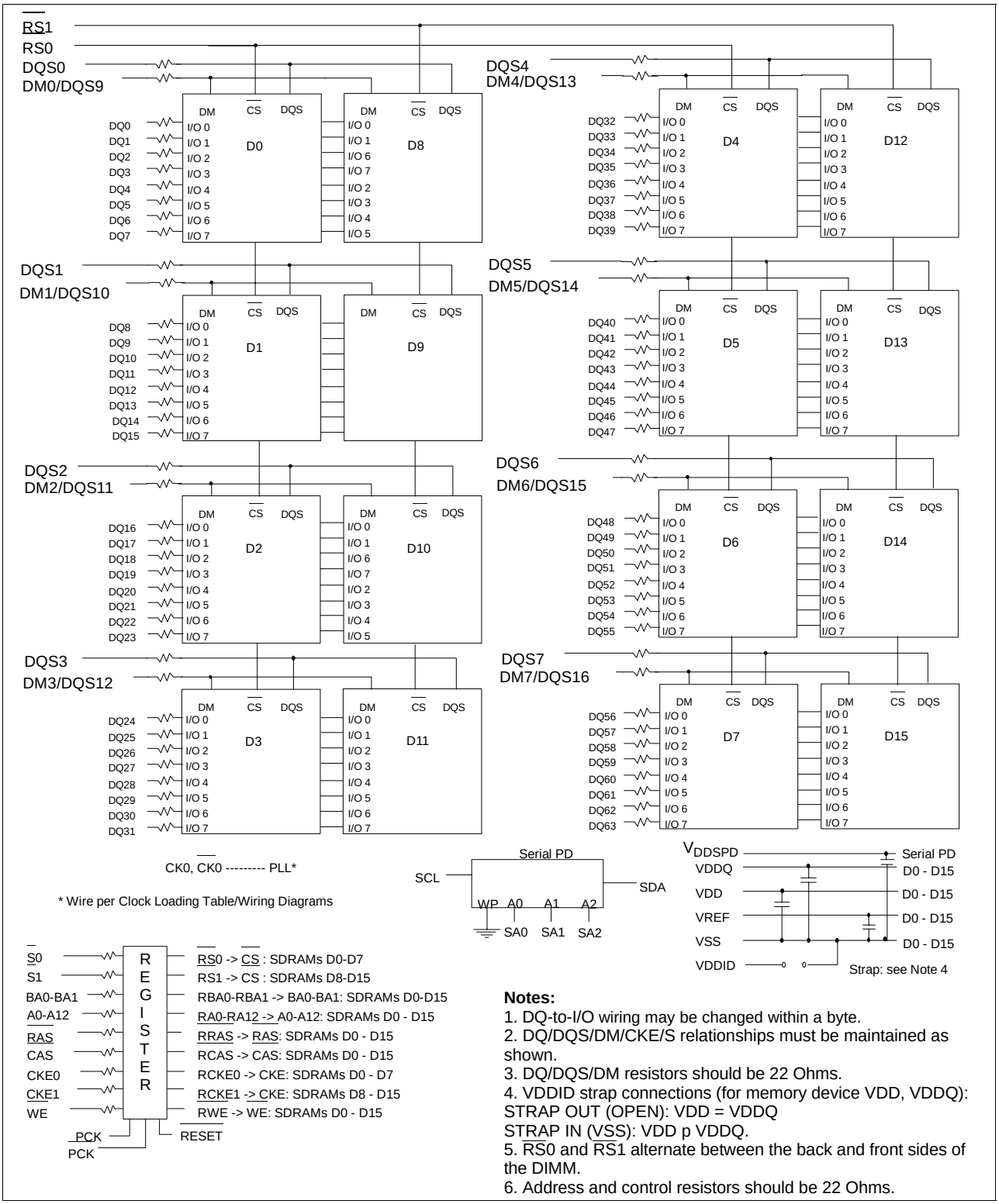


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

Block Diagram: Raw Card Version A

(x64 DIMM, populated as two physical banks of x8 DDR SDRAMs)

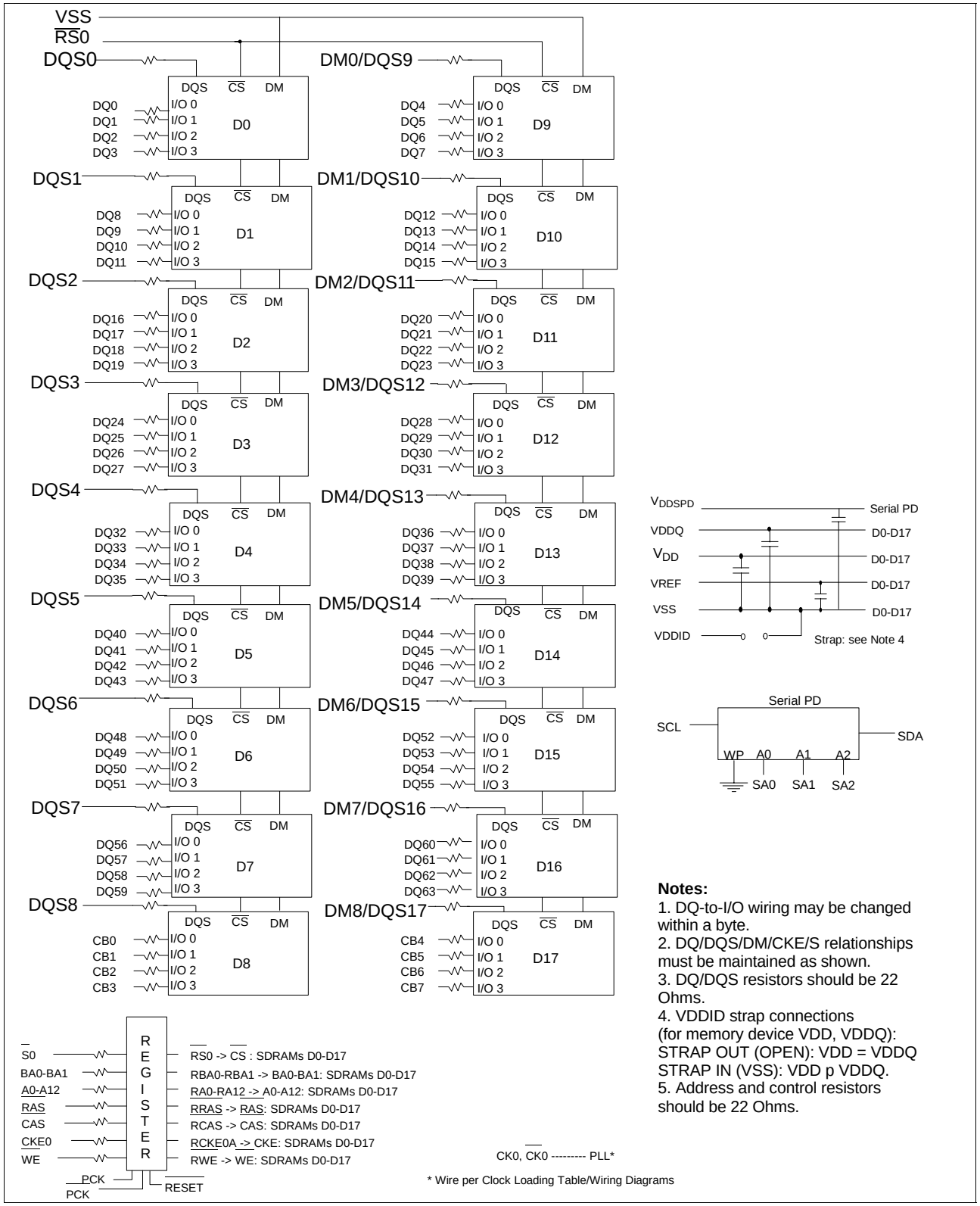


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD p VDDQ.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

Block Diagram: Raw Card Version B

(Populated as one physical bank of x4 DDR SDRAMs)

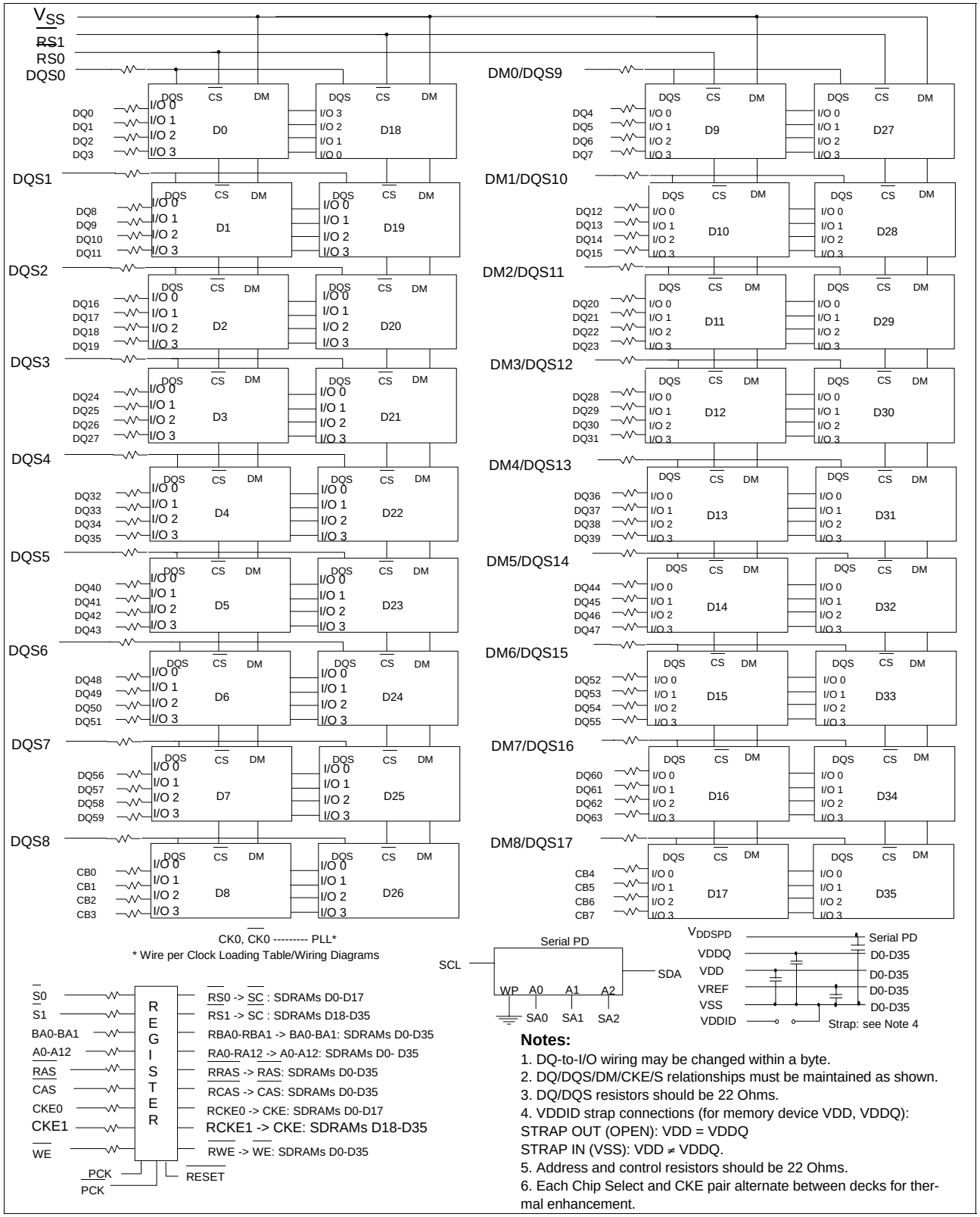


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ): STRAP OUT (OPEN): VDD = VDDQ STRAP IN (VSS): VDD p VDDQ.
5. Address and control resistors should be 22 Ohms.

Block Diagram: Raw Card Version C/E

(Populated as two physical banks of x4 DDR SDRAMs)

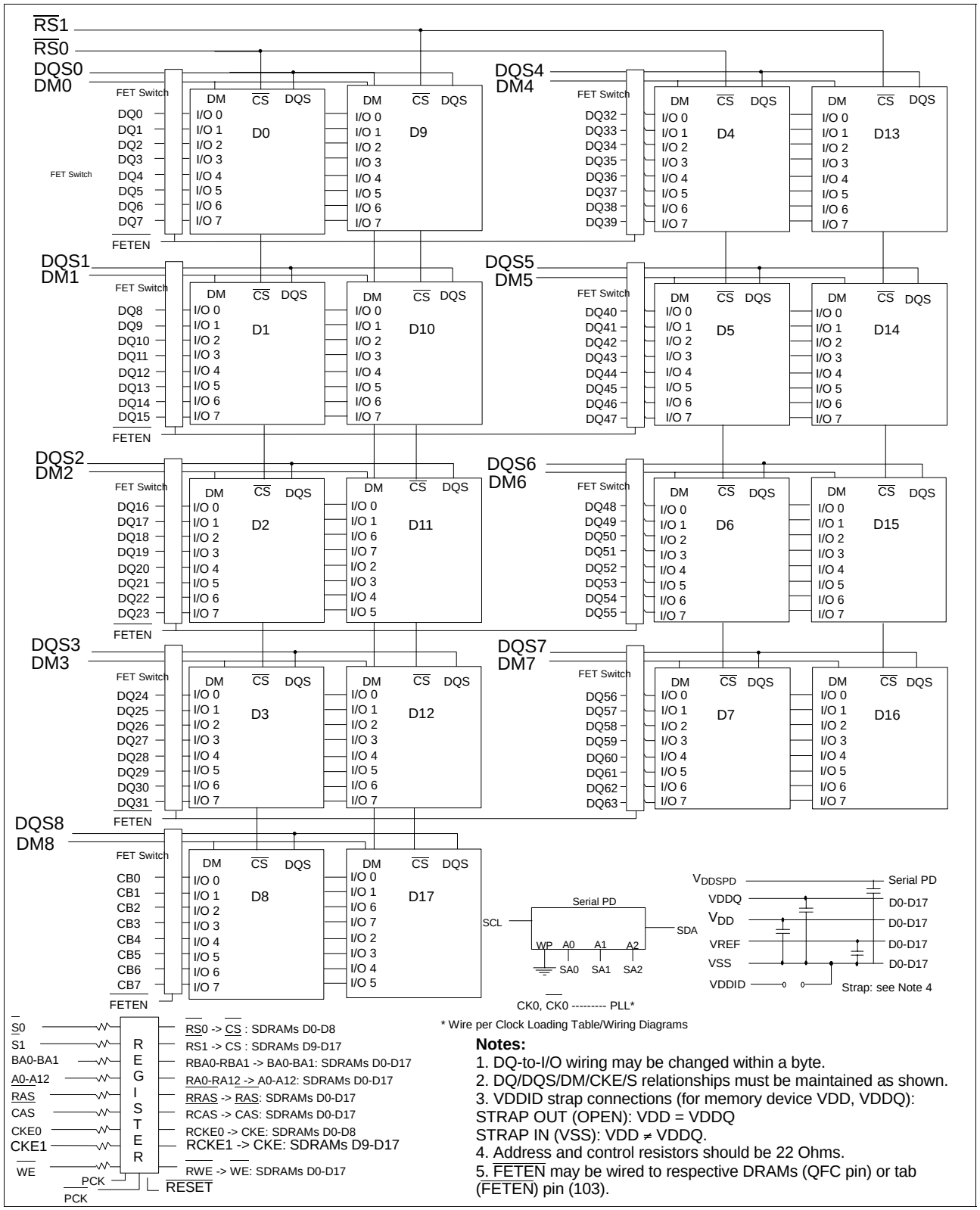


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

Block Diagram: Raw Card Version F

(x72 DIMM, populated as two physical banks of x8 DDR SDRAMs)



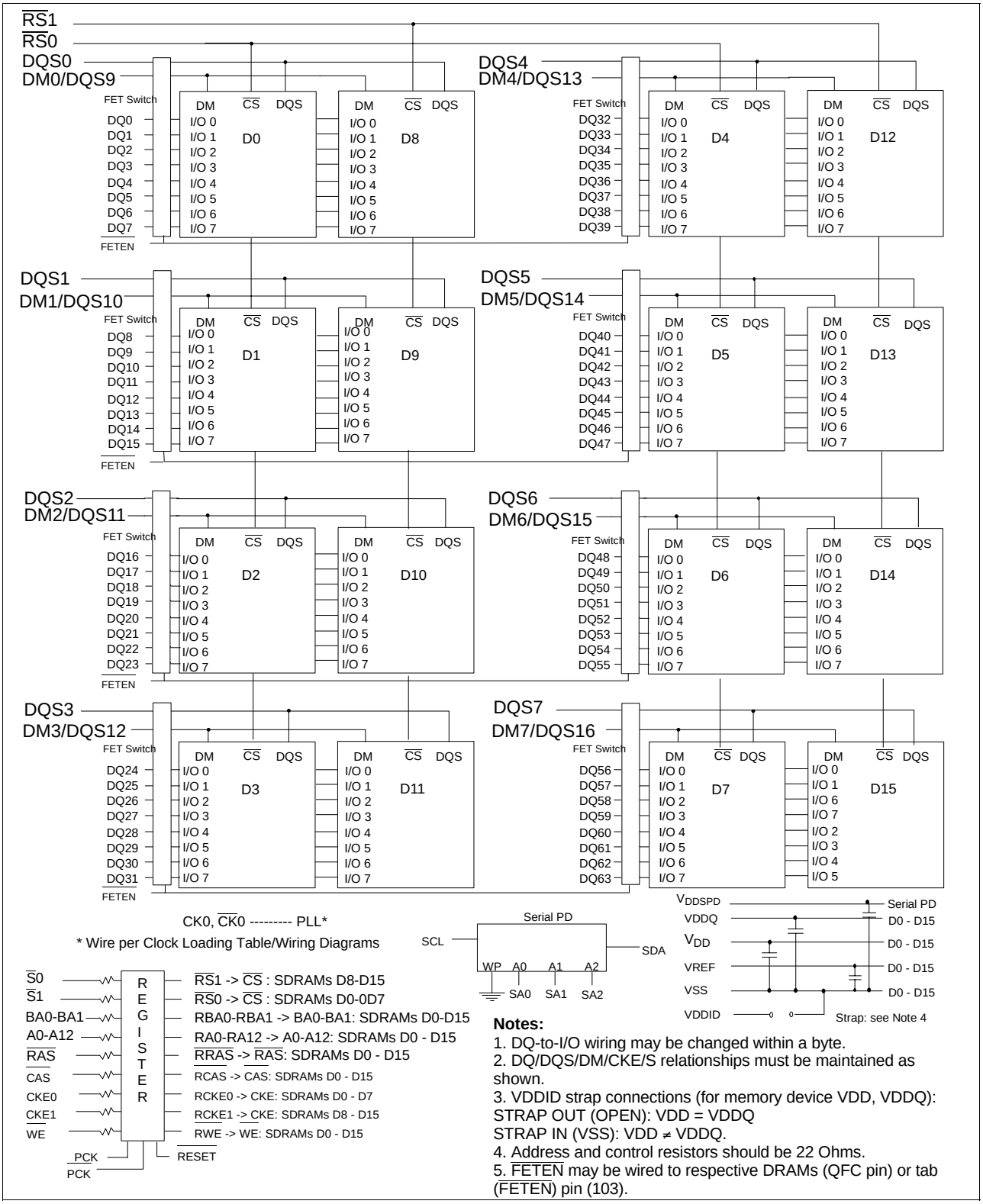
* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
4. Address and control resistors should be 22 Ohms.
5. FETEN may be wired to respective DRAMs (QFC pin) or tab (FETEN) pin (103).

Block Diagram: Raw Card Version F

(x64 DIMM, populated as two physical banks of x8 DDR SDRAMs)

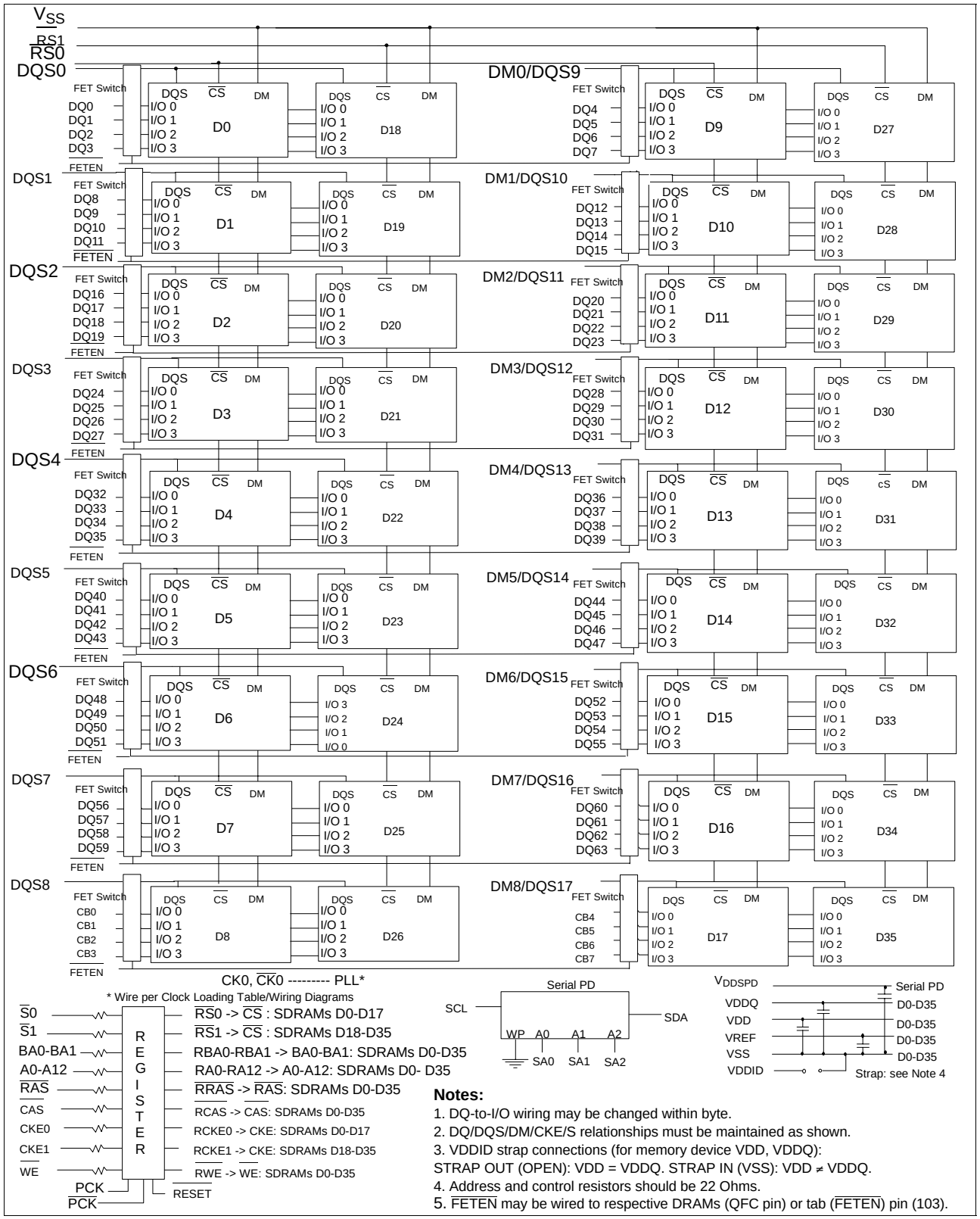


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
4. Address and control resistors should be 22 Ohms.
5. FETEN may be wired to respective DRAMs (QFC pin) or tab (FETEN) pin (103).

Block Diagram: Raw Card Version H/K

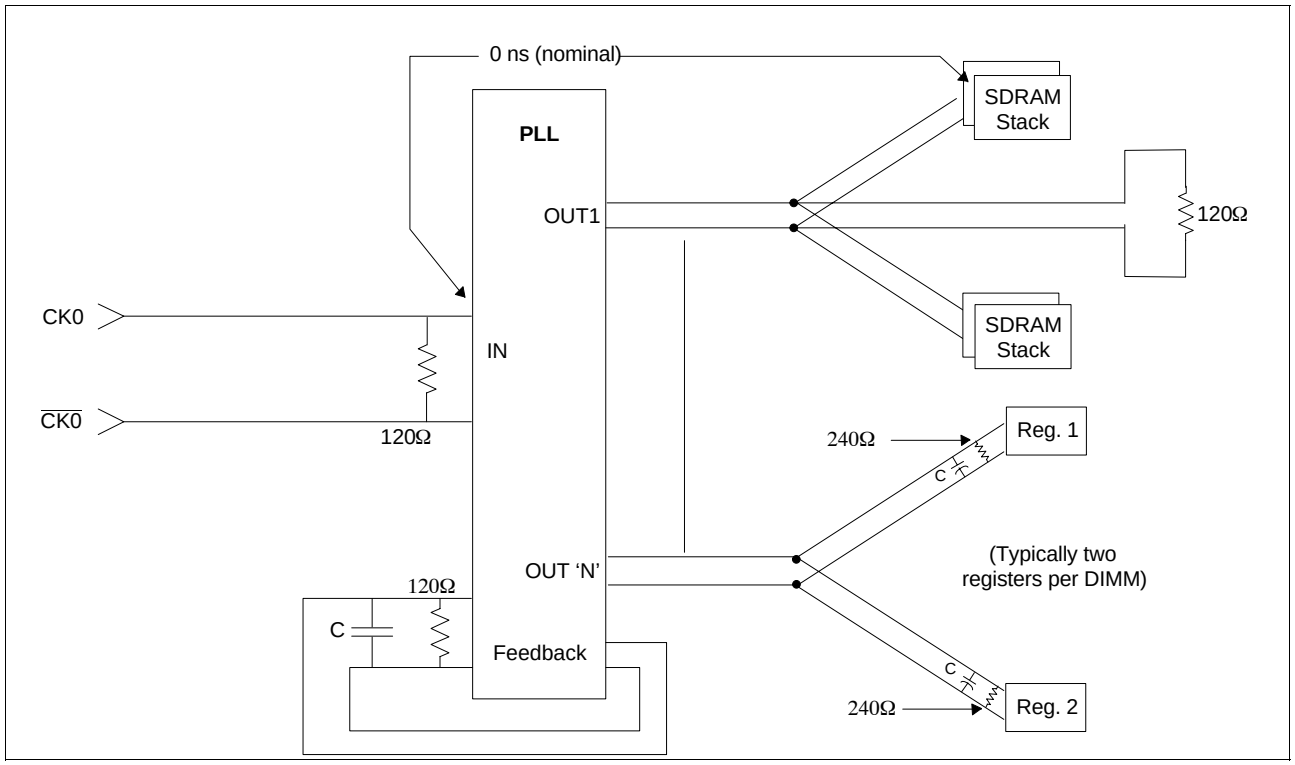
(x72 DIMM, populated as 2 physical banks of x4 DDR SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ. STRAP IN (VSS): VDD ≠ VDDQ.
4. Address and control resistors should be 22 Ohms.
5. FETEN may be wired to respective DRAMs (QFC pin) or tab (FETEN) pin (103).

Differential Clock Net Wiring (CK0, $\overline{CK0}$)



1. The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns (nominal). See “Clocking Timing Methodology” on page 57.
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.

Register Functional Assignments

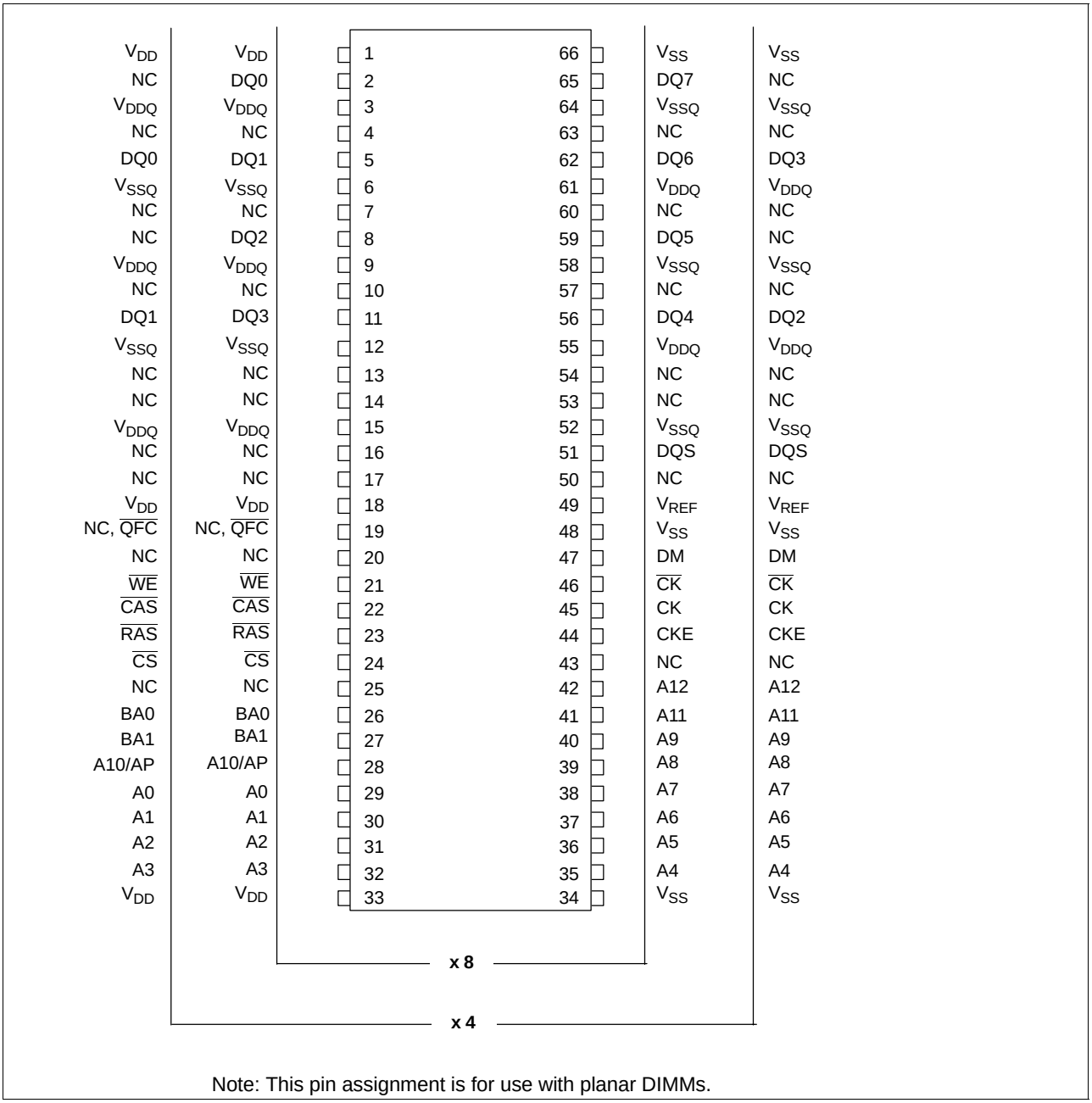
Raw Card Versions A, B, and F (Two 1:1 Registers)				Raw Card Versions C, E, H, and K (Two 1:2 Registers)			
Register 1		Register 2		Register 1		Register 2	
In	Out	In	Out	In	Out	In	Out
A1	RA1	A0	RA0	A1	RA1A	A0	RA0A
A2	RA2	A10	RA10		RA1B		RA0B
A3	RA3	$\overline{S}$0	$\overline{RS}$0	A2	RA2A	A10	RA10A
A4	RA4	$\overline{S}$1	$\overline{RS}$1		RA2B		RA10B
A5	RA5	$\overline{CAS}$	$\overline{RCAS}$	A3	RA3A	$\overline{S}$0	R$\overline{S0}$A
A6	RA6	$\overline{RAS}$	$\overline{RRAS}$		RA3B		R$\overline{S0}$B
A7	RA7	BA0	RBA0	A4	RA4A	$\overline{S}$1	R$\overline{S1}$A
A8	RA8	BA1	RBA1		RA4B		R$\overline{S1}$B
A9	RA9	$\overline{WE}$	$\overline{RWE}$	A5	RA5A	$\overline{CAS}$	R$\overline{CAS}$A
A11	RA11				RA5B		R$\overline{CAS}$B
A12[1]	RA12			A6	RA6A	$\overline{RAS}$	R$\overline{RAS}$A
CKE0	RCKE0				RA6B		R$\overline{RAS}$B
CKE1	RCKE1			A7	RA7A	BA0	RBA0A
					RA7B		RBA0B
				A8	RA8A	BA1	RBA1A
					RA8B		RBA1B
				A9	RA9A	$\overline{WE}$	R$\overline{WE}$A
					RA9B		R$\overline{WE}$B
				A11	RA11A		
					RA11B		
				A12[1]	RA12A		
					RA12B		
				CKE0	RCKE0A		
					RCKE0B		
				CKE1	RCKE1A		
					RCKE1B		

1. Only used with 256Mbit, 512Mbit SDRAMs

Component Details

Pin Assignments for 64Mb, 128Mb, 256Mb, and 512Mb DDR SDRAM Planar Components

(Top View)

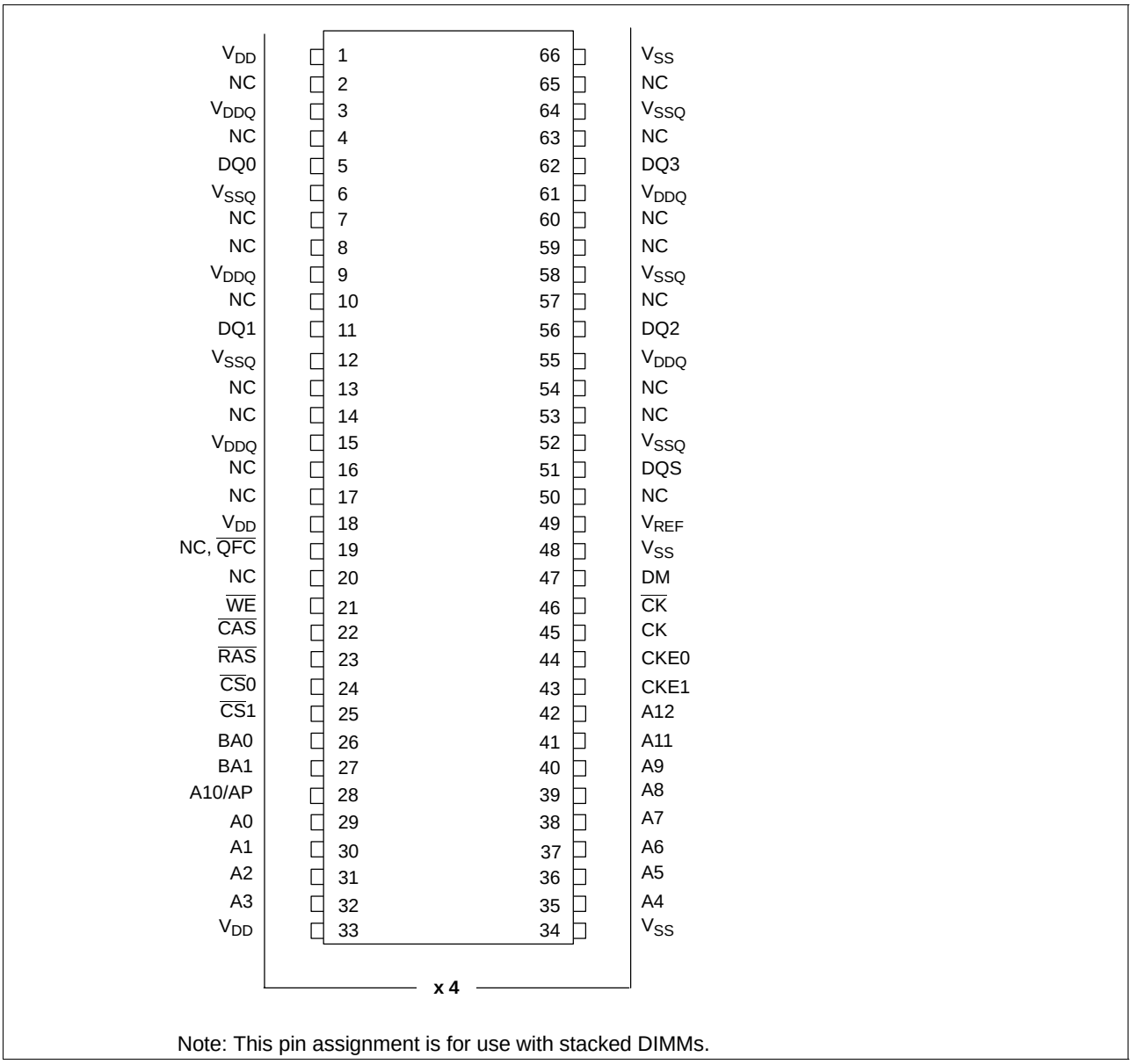


V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}
NC	DQ0	2	65	DQ7	NC
V_{DDQ}	V_{DDQ}	3	64	V_{SSQ}	V_{SSQ}
NC	NC	4	63	NC	NC
DQ0	DQ1	5	62	DQ6	DQ3
V_{SSQ}	V_{SSQ}	6	61	V_{DDQ}	V_{DDQ}
NC	NC	7	60	NC	NC
NC	DQ2	8	59	DQ5	NC
V_{DDQ}	V_{DDQ}	9	58	V_{SSQ}	V_{SSQ}
NC	NC	10	57	NC	NC
DQ1	DQ3	11	56	DQ4	DQ2
V_{SSQ}	V_{SSQ}	12	55	V_{DDQ}	V_{DDQ}
NC	NC	13	54	NC	NC
NC	NC	14	53	NC	NC
V_{DDQ}	V_{DDQ}	15	52	V_{SSQ}	V_{SSQ}
NC	NC	16	51	DQS	DQS
NC	NC	17	50	NC	NC
V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}
NC, $\overline{QFC}$	NC, $\overline{QFC}$	19	48	V_{SS}	V_{SS}
NC	NC	20	47	DM	DM
$\overline{WE}$	$\overline{WE}$	21	46	$\overline{CK}$	$\overline{CK}$
$\overline{CAS}$	$\overline{CAS}$	22	45	CK	CK
$\overline{RAS}$	$\overline{RAS}$	23	44	CKE	CKE
$\overline{CS}$	$\overline{CS}$	24	43	NC	NC
NC	NC	25	42	A12	A12
BA0	BA0	26	41	A11	A11
BA1	BA1	27	40	A9	A9
A10/AP	A10/AP	28	39	A8	A8
A0	A0	29	38	A7	A7
A1	A1	30	37	A6	A6
A2	A2	31	36	A5	A5
A3	A3	32	35	A4	A4
V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}

Note: This pin assignment is for use with planar DIMMs.

Pin Assignments for 64Mb, 128Mb, 256Mb, and 512Mb DDR SDRAM 2 High Stack Package

(Top View)



Note: This pin assignment is for use with stacked DIMMs.

DDR SDRAM Component Specifications

The DDR SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC ballots JC-42.3-98-227A. DDR SDRAM component specification violations also violate the DDR SDRAM Registered DIMM specifications.

Register Component Specifications

Please refer to the vendor register data sheets for all technical specifications and requirements. Below is a chart explaining which registers should be used on each DIMM type.

DIMM Register Use

Raw Card Version	# of Banks	# of SDRAMs per output	Register Type	Quantity
A	1	9	1:1 14-bit SSTL	2
	2	18	1:1 14-bit SSTL	2
B	1	18	1:1 14-bit SSTL	2
C/E	2	18	1:2 13-bit SSTL	2
F	2	18	1:1 14-bit SSTL	2
H/K	2	18	1:2 13-bit SSTL	2

The following specifications for the register are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on both the 1:1 and 1:2 registers, including driver characteristics, has been balloted at the JEDEC JC-40 Committee, Item #6 (1:1) and Item# 32 (1:2).

Critical Register Specifications

Register	Symbol	Parameter	Conditions	T_A = 0-70∞ C V_{DD} = 2.5V ± 0.2V		Units	Notes
				Min	Max		
1:1 14-bit and 1:2 13-bit	t_{CK}	Clock Frequency		60	170	MHz	
	t_{PD}	Clock to Output Time	30pF to GND and 50 Ohms to V_{TT}	1.1	2.8	ns	
	t_{RST}	Reset to Output Time		—	5	ns	
	t_{SL}	Output Slew Rate	30pF to GND and 50 Ohms to V_{TT}/2	0.5	4	V/ns	
	t_{su}	Setup time, fast slew rate (see Notes 1 and 3)		—	0.75	ns	1, 3
		Setup time, slow slew rate (see Notes 2 and 3)		—	0.9	ns	2, 3
	t_h	Hold time, fast slew rate (see Notes 1 and 3)			0.75		1, 3
		Hold time, slow slew rate (see Notes 2 and 3)			0.9		2, 3
	$C_{IN(CK)}$	Clock Input Capacitance		2.5	3.5	pF	
	$C_{IN(data)}$	Data Input Capacitance		2.5	3.5	pF	

1. For data signal, input slew rate ≥ 1 V/ns
2. For data signal, input slew rate ≥ 0.5 V/ns and < V/ns
3. For CLK and $\overline{CLK}$ signals, input slew rates are ≥ 1 V/ns.

Register Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM RDIMM registers meet the specifications documented above, it is up to each DIMM producer to select the registers and register vendors which meet these requirements, and to guarantee robustly designed DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of both the 1:1 and 1:2 registers have been balloted at JEDEC in JC-40, Item #6 (1:1) and Item# 32 (1:2).

PLL Component Specifications

Please refer to the vendor PLL data sheets for all technical specifications and requirements. Below is a chart explaining which PLLs are used on each DIMM type.

DIMM PLL Use

Raw Card Version	# of Banks	# of SDRAMs per output	PLL Type	Quantity
A	1	2[1]	1:10, 2.5 Volt	1
	2	2	1:10, 2.5 Volt	1
B	1	2	1:10, 2.5 Volt	1
C/E	2	4	1:10, 2.5 Volt	1
F	2	2	1:10, 2.5 Volt	1
H/K	2	4	1:10, 2.5 Volt	1

1. In the case of One–Bank A card, a padding capacitor is added across each SDRAM clock and $\overline{\text{clock}}$ pair to ensure that timing is the same for One and Two–Bank DIMMs. Also, on X64 A cards, a padding capacitor is used across the clock pair for the depopulated ninth SARAM(s) position(s).

The following specifications for the PLL are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on this part, including driver characteristics, has been balloted at the JEDEC JC-40 Committee, Item #25.

Critical PLL Specifications

Device	Symbol	Parameter	Conditions	T_A = 0-70∞ C V_{DD} = 2.5V ± 0.2V		Units	Notes
				Min	Max		
1:10, 2.5 Volt	f_{CK}	Operating Clock Frequency		60	170	MHz	1
	f_{CK}	Application Clock Frequency		95	170	MHz	1
	t_{SPE}	Static Phase Error	Application Load	-50	50	ps	2
	t_{SK}	Output Clock Skew	Application Load	—	100	ps	2
	t_{SL}	Output Slew Rate		1	3	V/ns	2
	t_{jit}(per)	Period		-75	75	ps	3, 4
	t_{jit}(cc)	Cycle-to-Cycle					
	t_{jit}(hper)	Half-period		-100	100		4
	t_{STAB}	PLL Stabilization Time			100	ms	
	C_{IN}	Input Capacitance		2.5	3.5	pF	

1. The PLL used on the registered DIMM needs to support SSC synthesizers with a Modulation Frequency of 30 to 50KHz and a Clock Frequency Deviation of –0.5%. PLL sedigns should target the fillowing values:
   - Greater than 1.2MHz PLL loop bandwidth
   - Less than -0.031 degrees of phase angle
2. The application load is defined in *Differential Clock Net Structures* on page 33
3. Period jitter defines the largest variation in clock period, around a nominal clock structure.
4. Period jitter and half–period jitter are independent from each other.

PLL Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM Registered DIMM PLLs meet the specifications documented above, it is up to each DIMM producer to select the PLL and PLL vendors which meet these requirements, and to guarantee robustly operating DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of this part have been balloted at JEDEC in JC-40, Item #25.

FET Switch Component Specification

Raw Cards F, H, and K are intended for use in applications requiring reduced DRAM data loading. FET switches are included on these DIMMs and are activated by the SDRAM devices, or by external control FETEN at DIMM connector pin 103. Plans for these devices and the DIMMs are not yet closed; details will be added to subsequent releases of this document.

Registered DIMM Details

DDR SDRAM Module Configurations (Reference Designs) Product Family

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
A	64MB	8Mx72	64Mbit	8Mx8	9	66 lead TSOP	1	4	12/9	No
	128MB	16Mx72	128Mbit	16Mx8	9	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	256Mbit	32Mx8	9	66 lead TSOP	1	4	13/10	No
	512MB	64Mx72	512Mbit	64Mx8	9	66 lead TSOP	1	4	13/11	No
	128MB	16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/9	No
	256MB	32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10	No
	512MB	64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10	No
	1GB	128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11	No
	64MB	8Mx64	64Mbit	8Mx8	8	66 lead TSOP	1	4	12/9	No
	128MB	16Mx64	128Mbit	16Mx8	8	66 lead TSOP	1	4	12/10	No
	256MB	32Mx64	256Mbit	32Mx8	8	66 lead TSOP	1	4	13/10	No
	512MB	64Mx64	512Mbit	64Mx8	8	66 lead TSOP	1	4	13/11	No
	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/9	No
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10	No
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10	No
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11	No
B	128MB	16Mx72	64Mbit	16Mx4	18	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	128Mbit	32Mx4	18	66 lead TSOP	1	4	12/11	No
	512MB	64Mx72	256Mbit	64Mx4	18	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	512Mbit	128Mx4	18	66 lead TSOP	1	4	13/12	No
C	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOP	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOP	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOP	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOP	2	4	13/12	No
E	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOJ	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOJ	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOJ	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOJ	2	4	13/12	No
F	128MB	16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/9	Yes
	256MB	32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10	Yes
	512MB	64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10	Yes
	1GB	128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11	Yes
	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/9	Yes
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10	Yes
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10	Yes
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11	Yes
G	Reserved									

DDR SDRAM Module Configurations (Reference Designs) Product Family

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
H	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOP	2	4	12/10	Yes
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOP	2	4	12/11	Yes
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOP	2	4	13/11	Yes
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOP	2	4	13/12	Yes
K	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOJ	2	4	12/10	Yes
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOJ	2	4	12/11	Yes
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOJ	2	4	13/11	Yes
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOJ	2	4	13/12	Yes

Input Loading Matrix

Signal Names	Input Device	Raw Card Version				
		A	B	C/E	F	H/K
Clock (CK0)	PLL	1	1	1	1	1
CKE0	Register	1	1	1	1	1
CKE1	Register	1 or 0	N/A	1	1	1
Addr/RAS/CAS/BA/WE	Register	1	1	1	1	1
Chip Selects	Register	1	1	1	1	1
DQ/DQS	DDR SDRAM	1 or 2	1	2	0 or 2[1]	0 or 2[1]
	FET Switch	N/A	N/A	N/A	1	1
DM	DDR SDRAM	1 or 2	N/A	N/A	0 or 2[1]	N/A
	FET Switch	N/A	N/A	N/A	1	1
SCL/SDA/SA	EEPROM	1	1	1	1	1

1. FET switches are enabled and disabled during DIMM operation and thus the load changes.

DDR Registered Design File Releases

'Reference' Design file updates will be released as needed. This Registered DIMM specification will reflect the most recent Design files, but may also be updated to reflect clarifications to the specification only; in these cases the Design files will not be updated. The following table outlines the most recent Design file releases.

Note: Future Design file releases will include both a date and a revision label. All changes to the Design file are also documented in detail within the 'read-me' file.

Raw Card Version	Specification Revision	Applicable Design File	Notes
A	0.6	A0	Release on 12/15/99
	1.0	A1	Release on 03/31/00
B	0.6	B1	Release on 11/26/99
	1.0	B2	Release on 03/31/00
C	0.9[1]	C1	Release on 02/25/00
	0.95 (JEDEC ballot)	C2[2]	Release on 06/23/00
	1.0	C3[2]	Release on 08/01/00
E	1.0	TBD	Original Release
F	1.0	TBD	Original Release
H	1.0	TBD	Original Release
K	1.0	TBD	Original Release

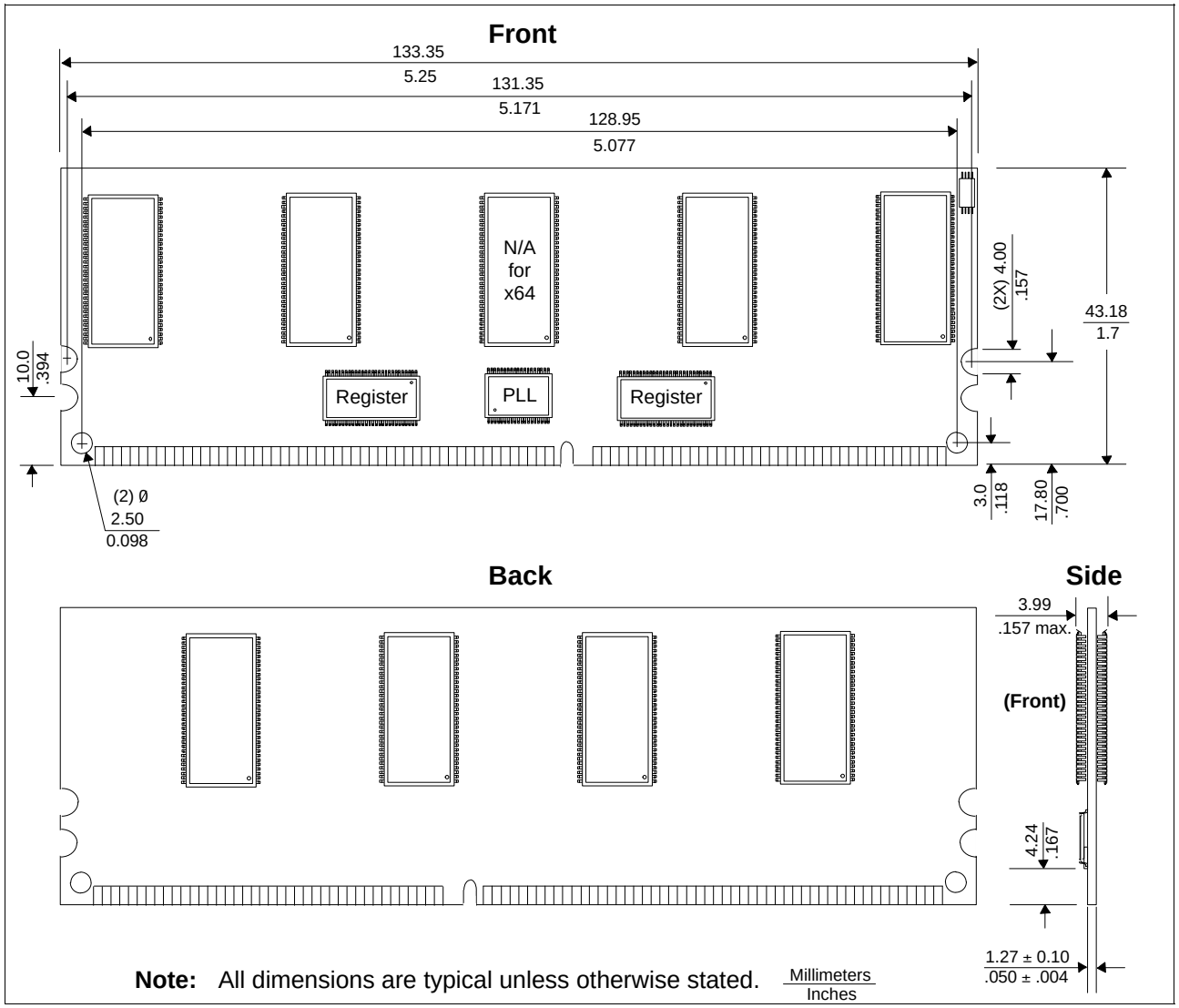
1. With exception of the cross section which utilized Revision 0.6
2. The C2 release is missing the gnd via connection for impedance coupons. The C3 release corrects this error. The omission has no bearing on the use of this design level in systems applications.

Component Types and Placement

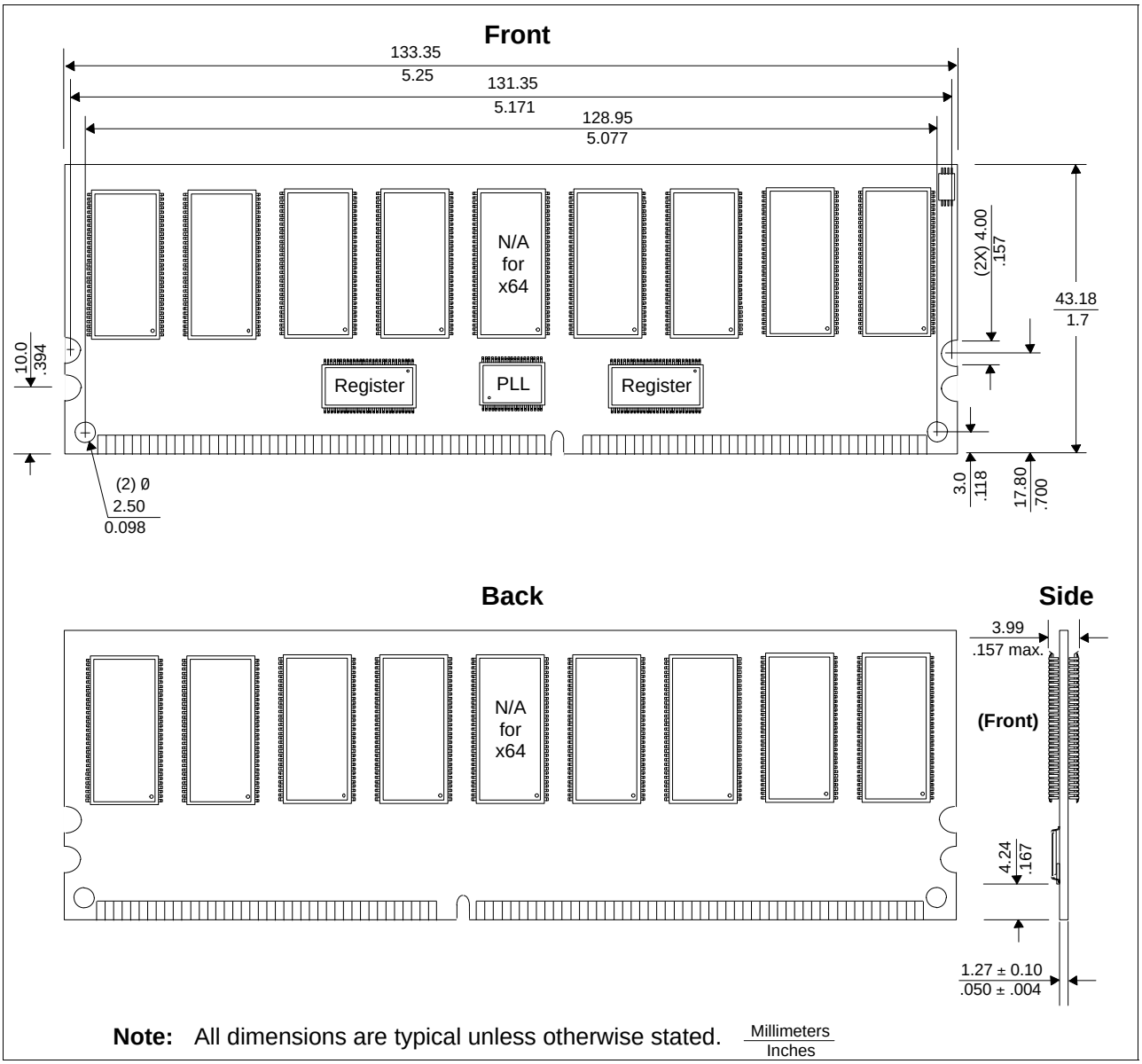
Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins. In two-bank, x4 based DDR SDRAM designs, the second DDR SDRAM bank devices will be stacked on the first DDR SDRAM bank devices.

The following layouts suggest placement for the Raw Card Versions A, B, C, E, F, H, and K. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

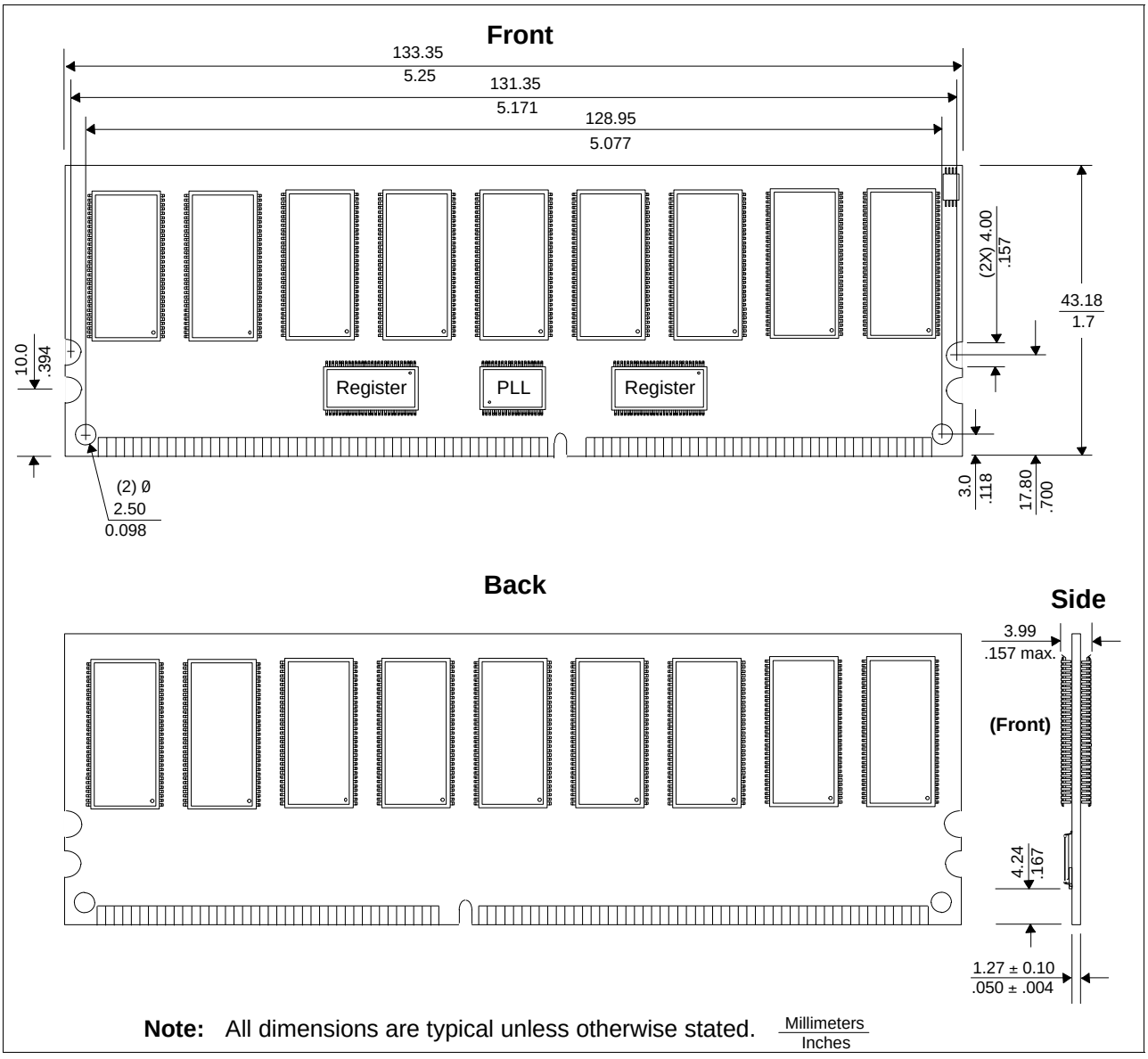
Example Raw Card Versions A (1 Physical Bank) Component Placement



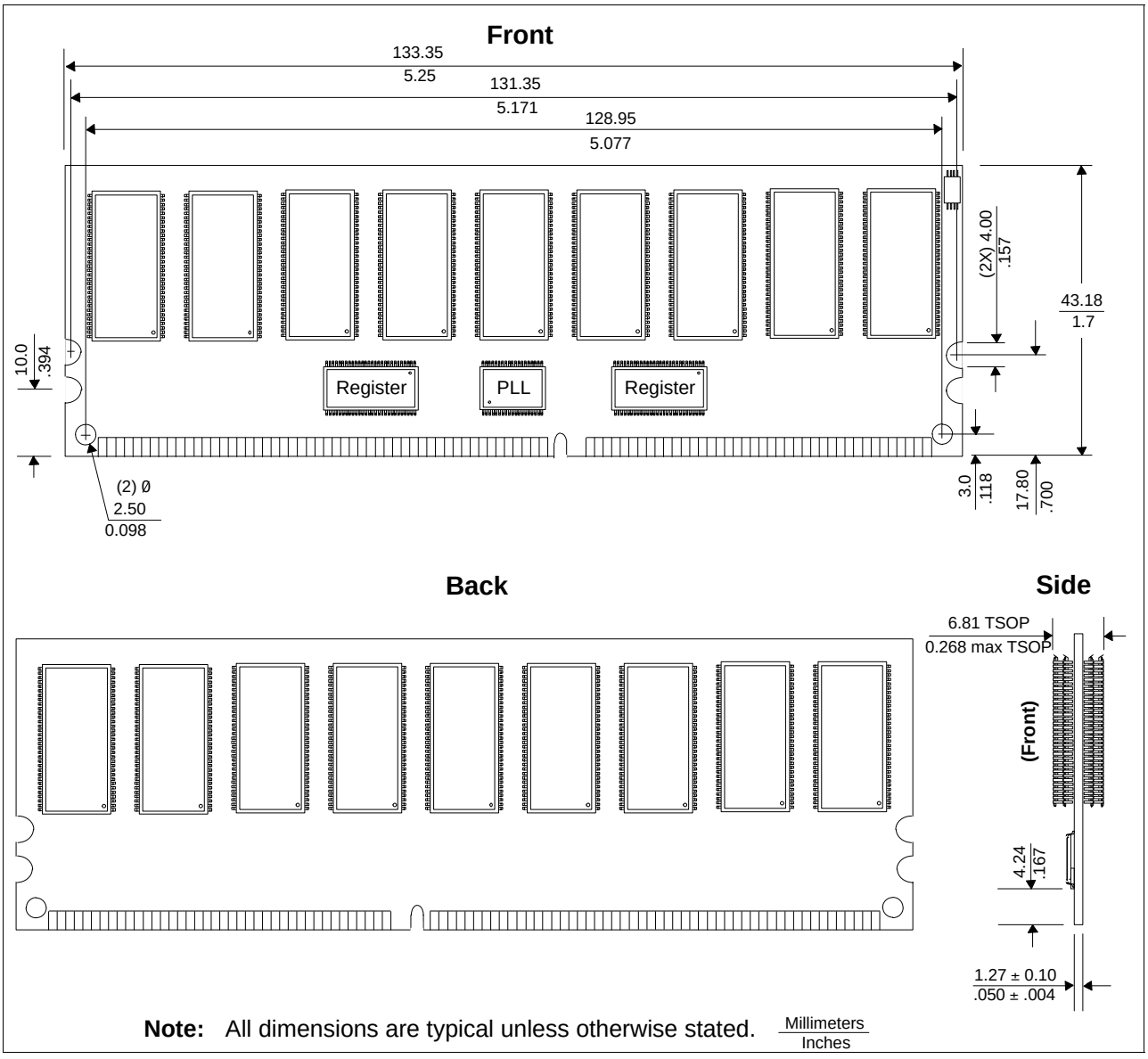
Example Raw Card Versions A (2 Physical Banks) Component Placement



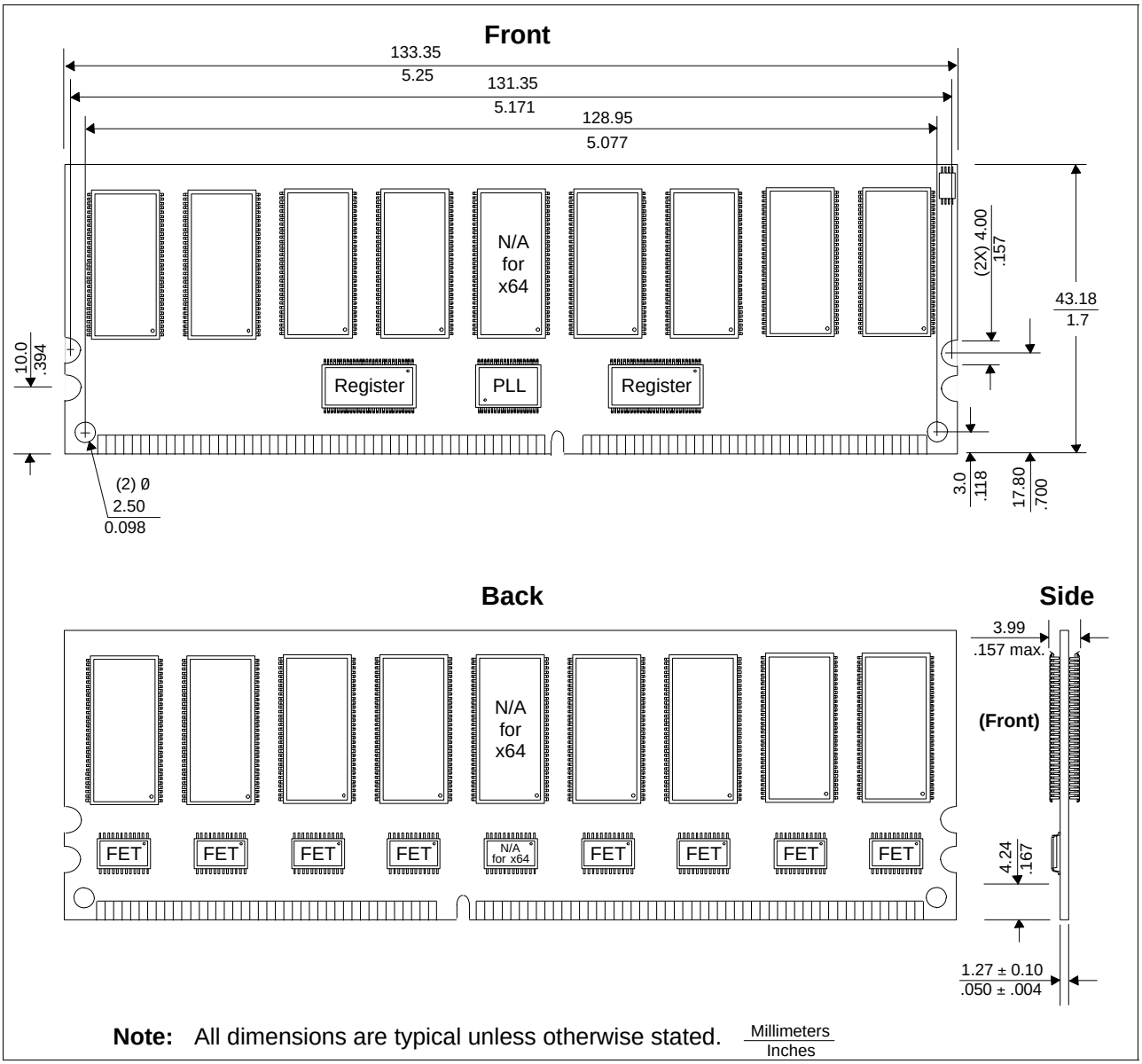
Example Raw Card Version B Component Placement



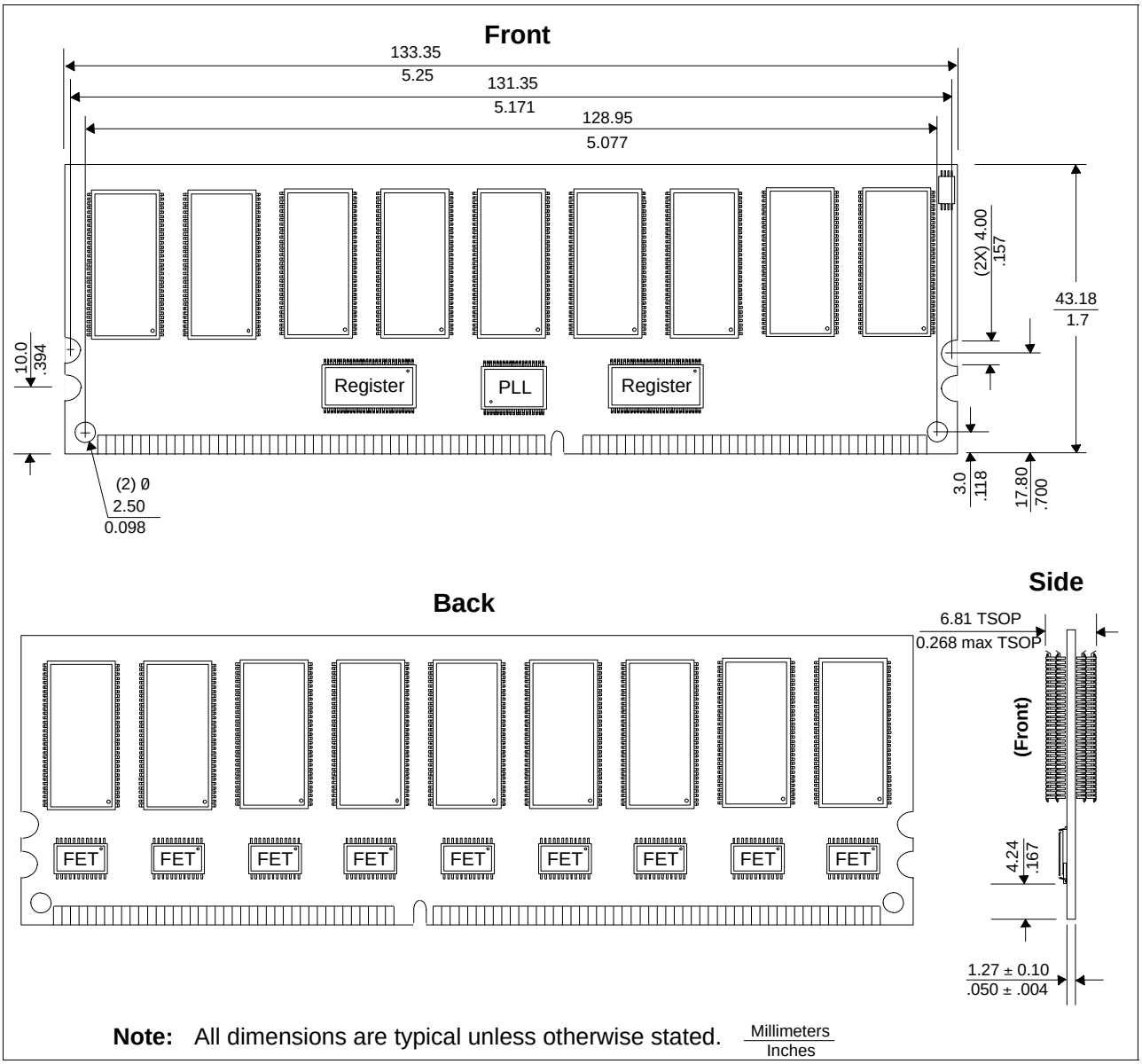
Example Raw Card Version C/E Component Placement



Example Raw Card Version F Component Placement



Example Raw Card Versions H and K Component Placement



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

DIMM Wiring Details

Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into seven groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Page
PLL Input / Unused Clocks	CK. $\overline{CK}$	A, B, C, E, F, H, K	33
PLL Output	PCK[9:0]	A, B, C, E, F, H, K	34-35
Data	DQ[63:0], CB[7:0]	B, C, E	36
		A	36, 37
		H/K	38
		F	38
DQS	DQS[17:0]	B, C, E	36-37
		A	36-37
		H/K	38
		F	38
DM	DM[8:0]	A	37
		F	39
Address and Control	A[12:0], BA[1:0], RAS, CAS, WE	A, B, F	40, 41
	A[12:0], BA[1:0], RAS, CAS, WE	C, E, H, K	46, 47
Chip Select, Clock Enable	$\overline{CS}$[0:1], CKE [0:1]	A, F	42, 43
		B	44, 45
		C, E, H, K	48, 49

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows

- Route all signal traces except clocks using 4/6 rules, i.e., 4 mil traces and 6 mil minimum spacing between adjacent traces.
- Route clocks using 4 mil lines and 6 mil spaces between differential clock pairs.
- Route clocks using at least 90% of the total trace length in the inner layers.

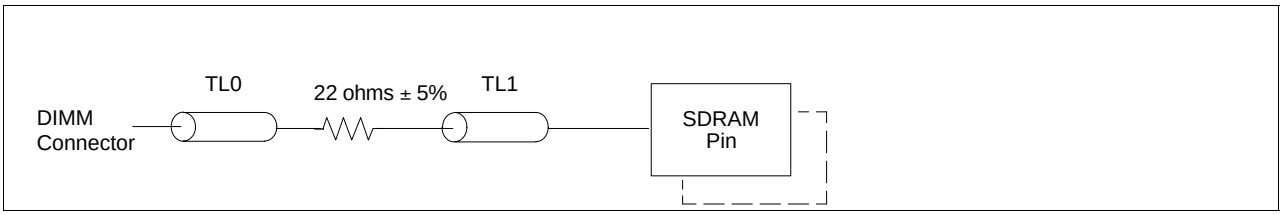
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 512MB double-sided x72 DIMM using 128Mbit, 32Mx4 SDRAM devices would have a data net structure as shown in the following diagram.



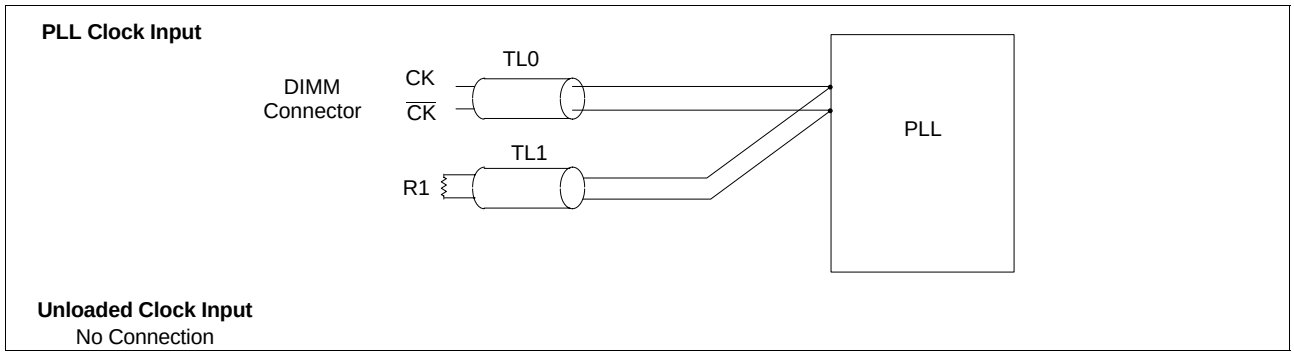
Differential Clock Net Structures

CK, $\overline{CK}$

DDR SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 100 mils total) between clocks of the same function
- PLL input net segment length is newly defined and optimized for high speed DDR Registered DIMMs.

Net Structure for PLL Input

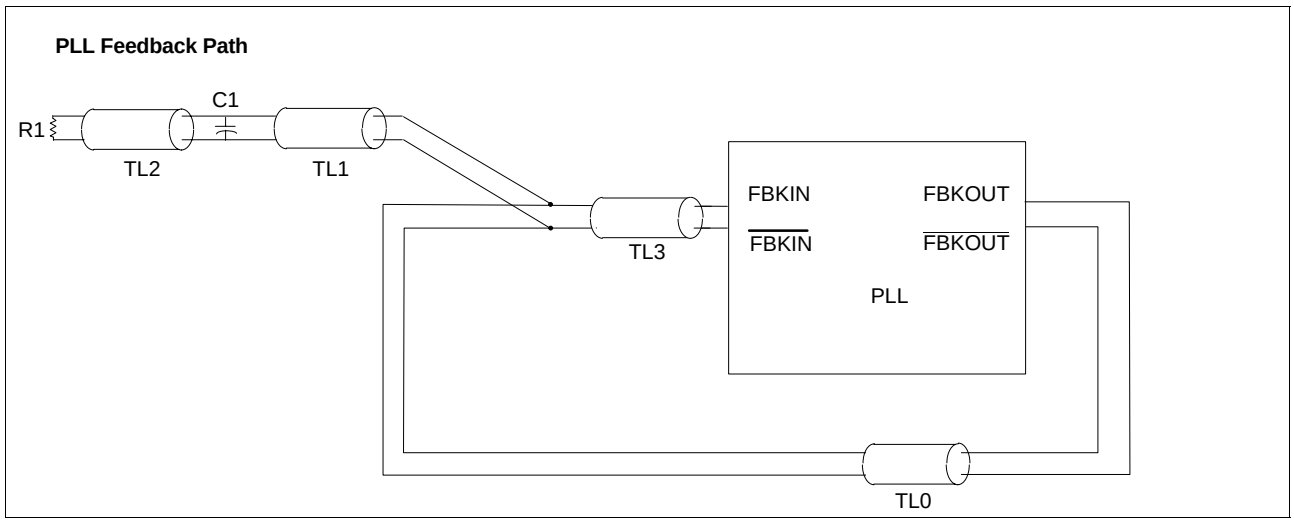


Clock Net Lengths for PLL Input Net Structures

Raw Card	TL0	TL1	R1 (Ohms)	Notes
A, B, C, E, F, H, K	1.00	0.20	120	1, 2, 3

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%
3. The termination resistor and loading capacitor are both placed after the pin of the PLL.

Net Structure Routing for PLL Feedback Path

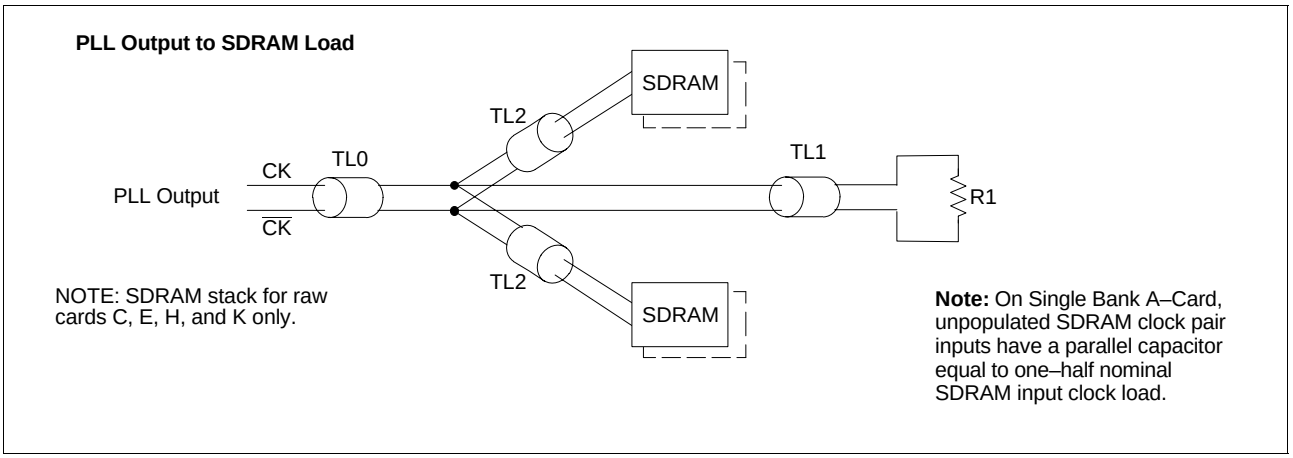


Trace Lengths for PLL Feedback Path Net Structure

Raw Card	TL0		TL1	TL2	TL3		R1 (Ohms)	C1 [pF]	Notes
	Min	Max			Min	Max			
A, B, F	2.92	3.02	0.04	0.29	0.05	0.09	120	Not populated	1, 2, 3
C, E, H, K	2.93	3.02	0.04	0.29	0.05	0.09	120	5.6	1, 2, 3

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%
3. The termination resistor and loading capacitor are both placed after the pin of the PLL.

Net Structure Routing for PLL Output to SDRAM Load



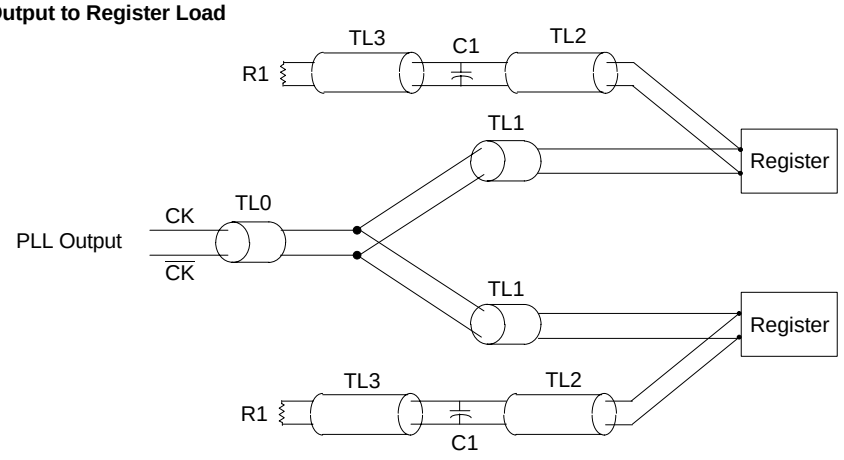
Trace Lengths for PLL Clock Output to SDRAM Load Net Structure

Raw Card	TL0		TL1		TL2		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max		
A	2.46	2.50	0.49	0.58	0.29	0.30	120	1, 2
B	2.46	2.49	0.49	0.57	0.29	0.31	120	1, 2
C/E	2.51	2.52	0.57	0.57	0.29	0.31	120	1, 2
F	TBD	TBD	TBD	TBD	TBD	TBD	120	1, 2
H/K	TBD	TBD	TBD	TBD	TBD	TBD	120	1, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%

Net Structure Routing for PLL Output to Register Load

PLL Output to Register Load



Unloaded PLL Output

All PLL outputs are used in each design.

Trace Lengths for PLL Clock Output to Register Load Net Structure

Raw Card	TL0		TL1		TL2		TL3		R1 [Ohms[	C1 [pF]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max			
A	0.05	0.05	2.71	2.72	0.13	0.15	0.07	0.07	240	Not populated	1, 2
B	0.05	0.05	2.71	2.72	0.13	0.15	0.07	0.07	240	Not populated	1, 2
C/E	0.05	0.05	3.51	3.51	0.13	0.14	0.07	0.07	240	Not populated	1, 2
F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	240	Not populated	1, 2
H/K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	240		1, 2

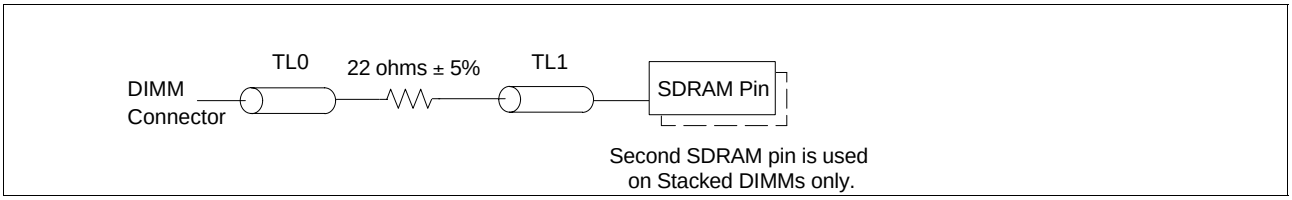
1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%

Data Net Structures

DQ[63:0], CB[7:0]
DQS[17:0]

Special attention has been paid to balancing data nets within a DDR SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. We recommend consistent delays for all nets, as described in the following tables.

Net Structure Routing for Data and DQS (Raw Cards B, C, and E)



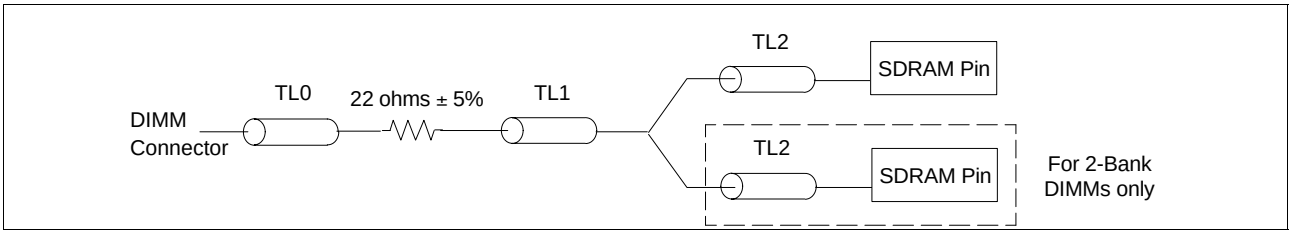
Trace Lengths for Data and DQs Net Structure (Raw Cards B, C, and E)

Raw Card	TL0		TL1		Total		Notes
	Min	Max	Min	Max	Min	Max	
B	0.13	0.19	0.95	1.02	1.13	1.14	1, 2
C/E	0.13	0.19	0.95	1.02	1.13	1.15	1, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%

DQ[63:0], CB[7:0]
DQS[8:0]

Net Structure Routing for Data and DQS (Raw Card A)



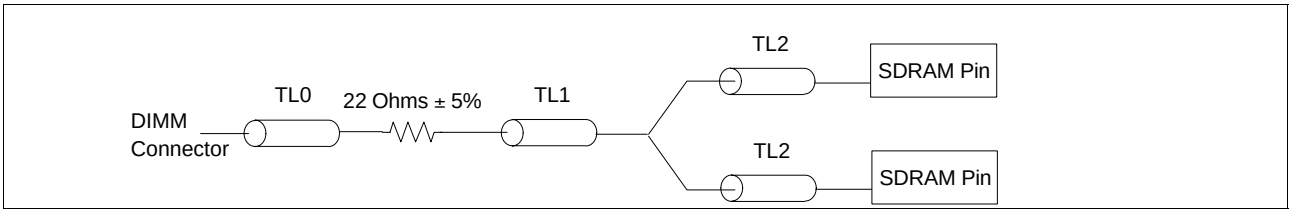
Trace Lengths for Data and DQS Net Structure (Raw Card A)

Raw Card	TL0		TL1		TL2		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A	0.13	0.19	0.59	0.65	0.37	0.37	1.15	1.15	42, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1

DM[8:0]

Net Structure Routing for DM (Raw Card A)



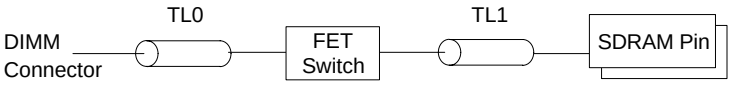
Trace Lengths for DM Net Structure (Raw Card A)

Raw Card	TL0		TL1		TL2	Total		Notes
	Min	Max	Min	Max		Min	Max	
A	0.13	0.19	0.67	0.69	0.44	1.25	1.30	1, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1

DQ[63:0], CB[7:0]
DQS [17:0]

Net Structure Routing for Data and DQS (Raw Cards H and K)



Second SDRAM pin is used
on Stacked DIMMs only.

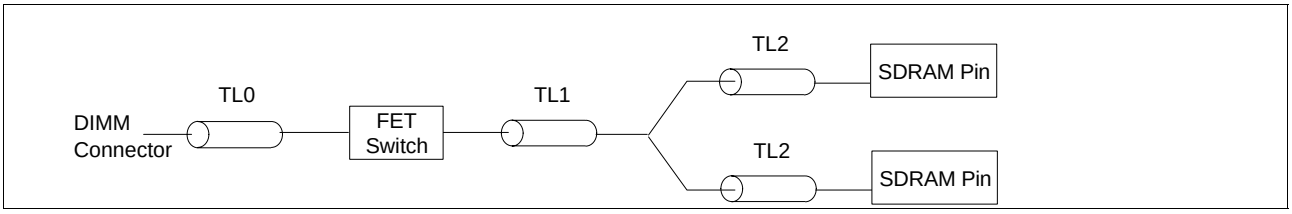
Trace Lengths for Data and DQS Net Structure (Raw Cards H and K)

Raw Card	TL0		TL1		Total		Notes
	Min	Max	Min	Max	Min	Max	
H	TBD	TBD	TBD	TBD	TBD	TBD	1, 2
K	TBD	TBD	TBD	TBD	TBD	TBD	1, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1

DQ [63:0], CB [7:0]
DQS[8:0]

Net Structure Routing for Data and DQS (Raw Card F)



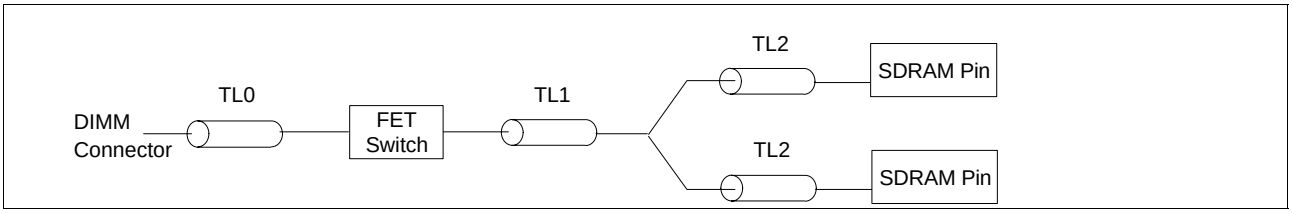
Trace Lengths for Data and DQS Net Structure (Raw Card F)

Raw Card	TL0		TL1		TL2		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	1, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1

DM[8:0]

Net Structure Routing for DM (Raw Card F)



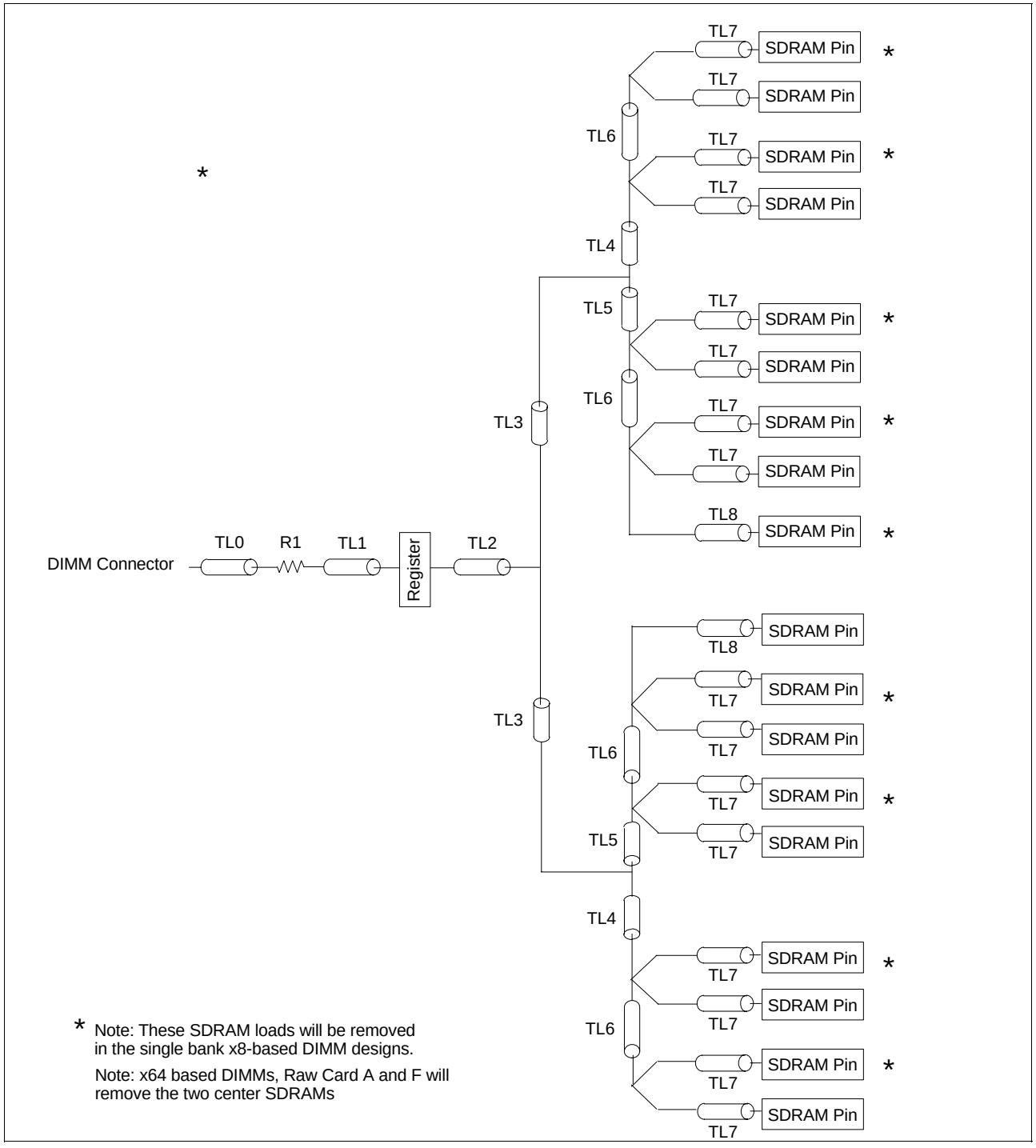
Trace Lengths for DM Net Structure (Raw Card F)

Raw Card	TL0		TL1		TL2		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	1, 2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1

Trace Lengths for Address and Control Net Structure (Raw Cards A, B, and F)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Control Net Structure (Raw Cards A, B, and F)

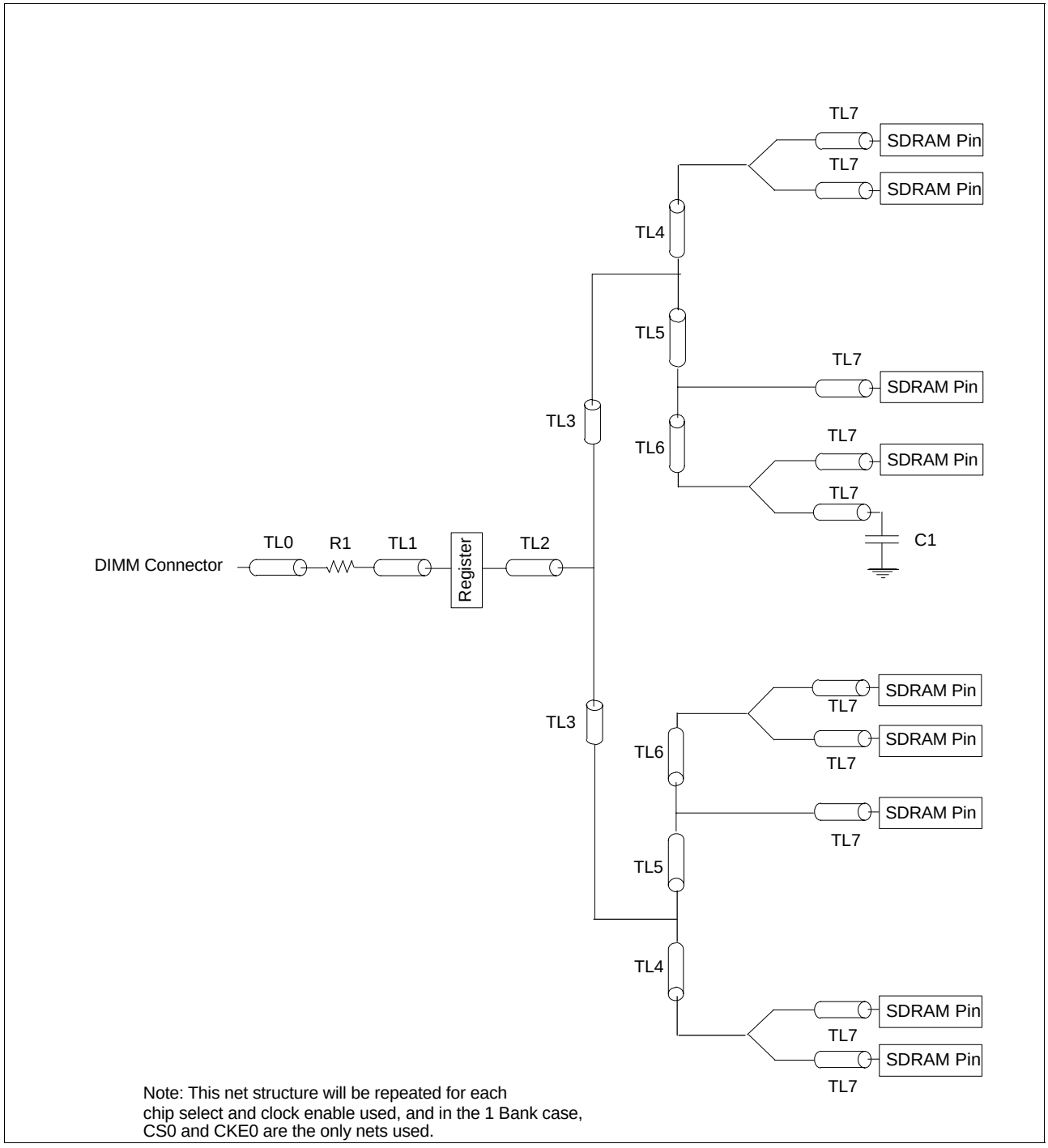
A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 [Ohms]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	0.13	0.26	0.56	0.66	0.62	1.37	1.39	2.57	0.40	0.56	0.14	0.15	0.48	0.63	0.20	0.32	0.49	0.72	22	1
B	0.13	0.28	0.54	0.67	0.66	1.38	1.31	2.55	0.40	0.53	0.12	0.15	0.50	0.64	0.20	0.29	0.49	0.72	22	
F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for $\overline{CS}$ and CKE (Raw Cards A and F)

$\overline{CS}$ [1:0], CKE [1:0]



Trace Lengths for $\overline{CS}$ and CKE (Raw Cards A and F)

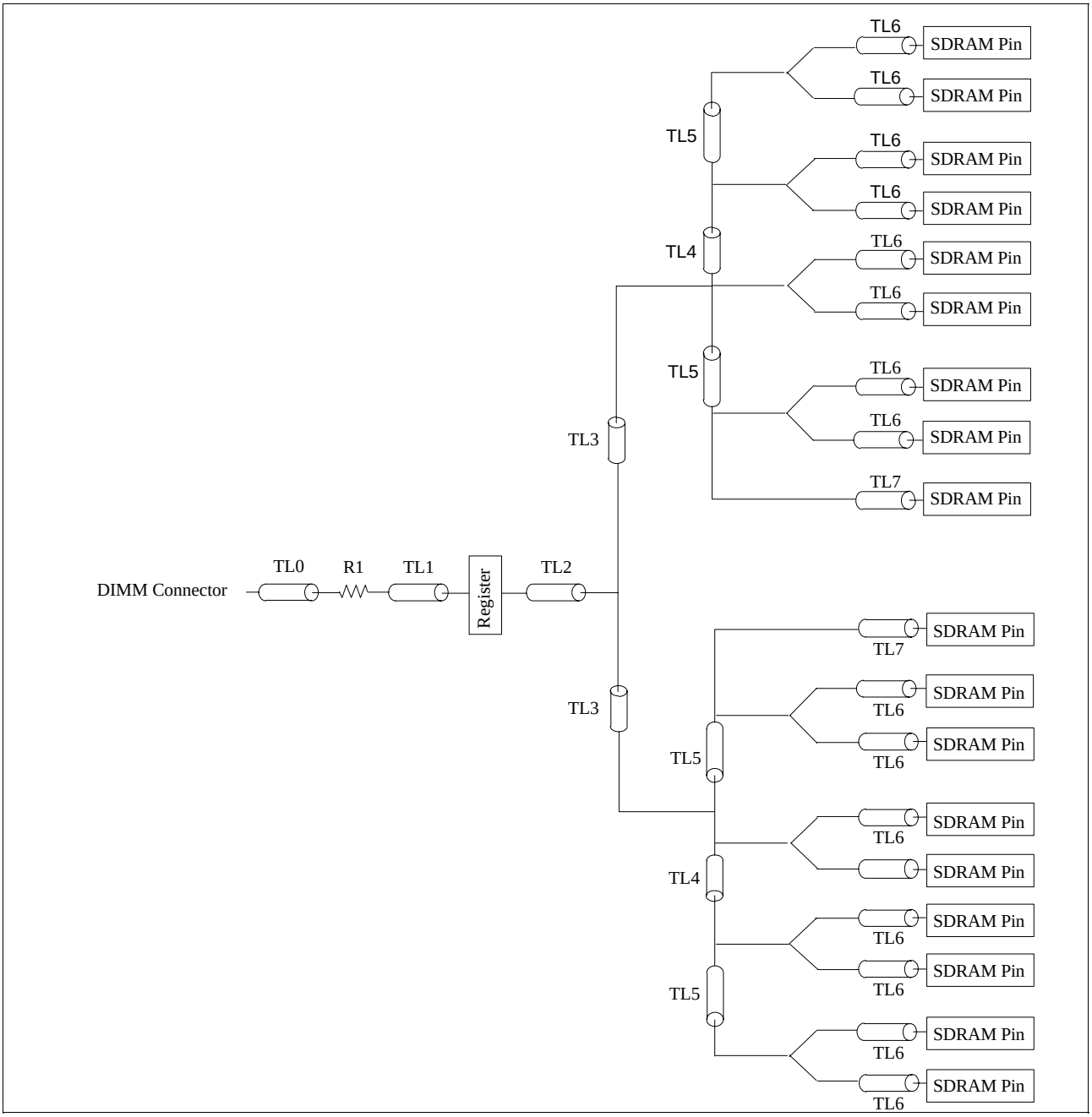
$\overline{CS}$ [1:0], CKE [1:0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		C1 [pF]	R1 [Ohms]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
A	0.12	0.21	0.60	0.65	1.16	1.43	1.67	2.10	0.15	0.28	0.53	0.69	0.23	0.77	0.08	0.78	3.0	22	1
F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch

Net Structure Routing for $\overline{CS}$ and CKE (Raw Card B)

$\overline{CS}$ [0], CKE [0]



Trace Lengths for CS and CKE (Raw Card B)

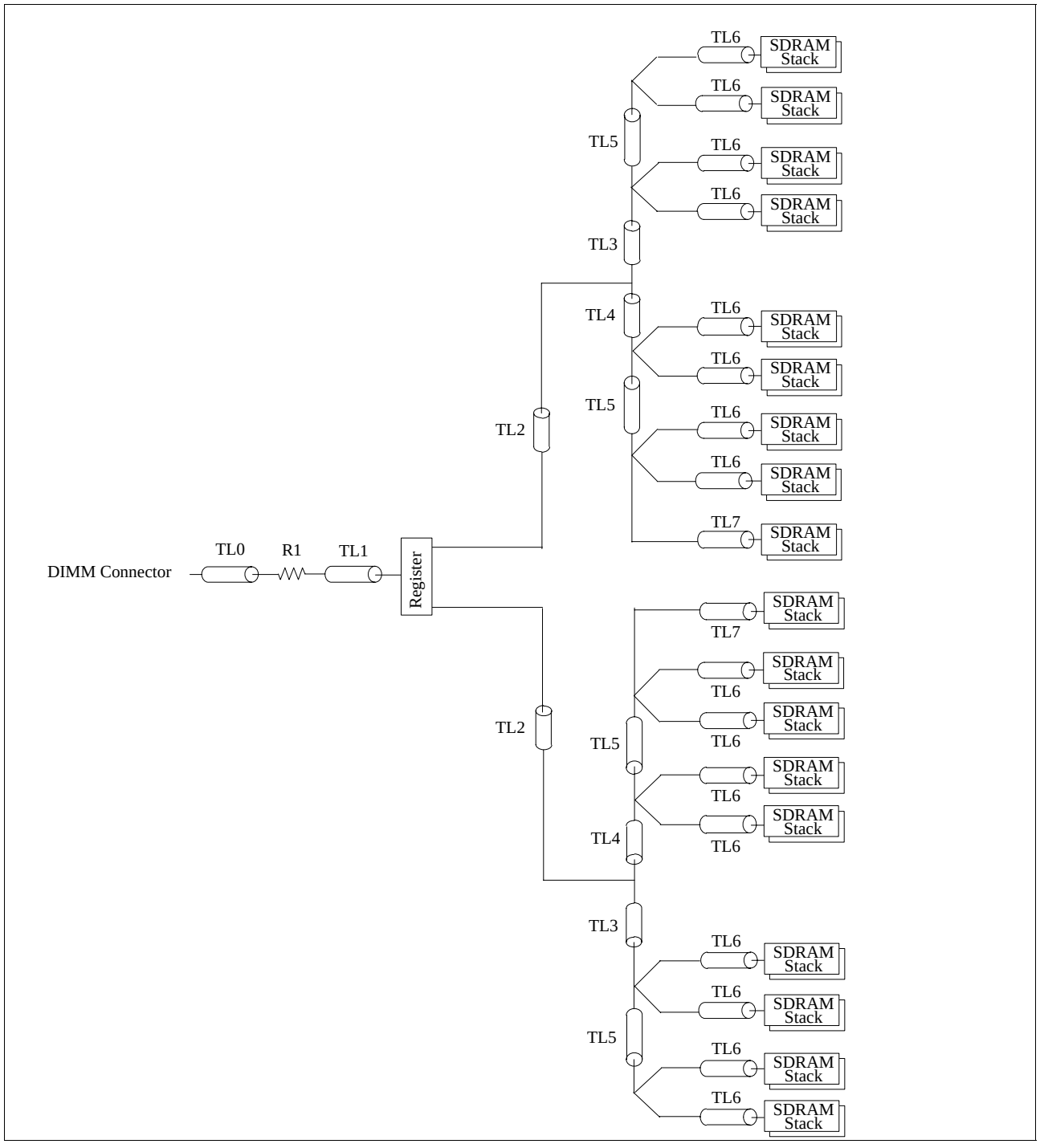
$\overline{CS}$[1:0], CKE[1:0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 [Ohms]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.13	0.16	0.612	0.65	1.17	1.23	1.43	1.68	0.58	0.72	0.40	0.58	0.15	0.35	0.56	0.76	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch

Net Structure Routing for Address and Control (Raw Cards C, E, H, and K)

$\overline{CS}$[0:1], CKE[0:1]BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



Trace Lengths for Address and Control Net Structure (Raw Card C, E, H, and K)

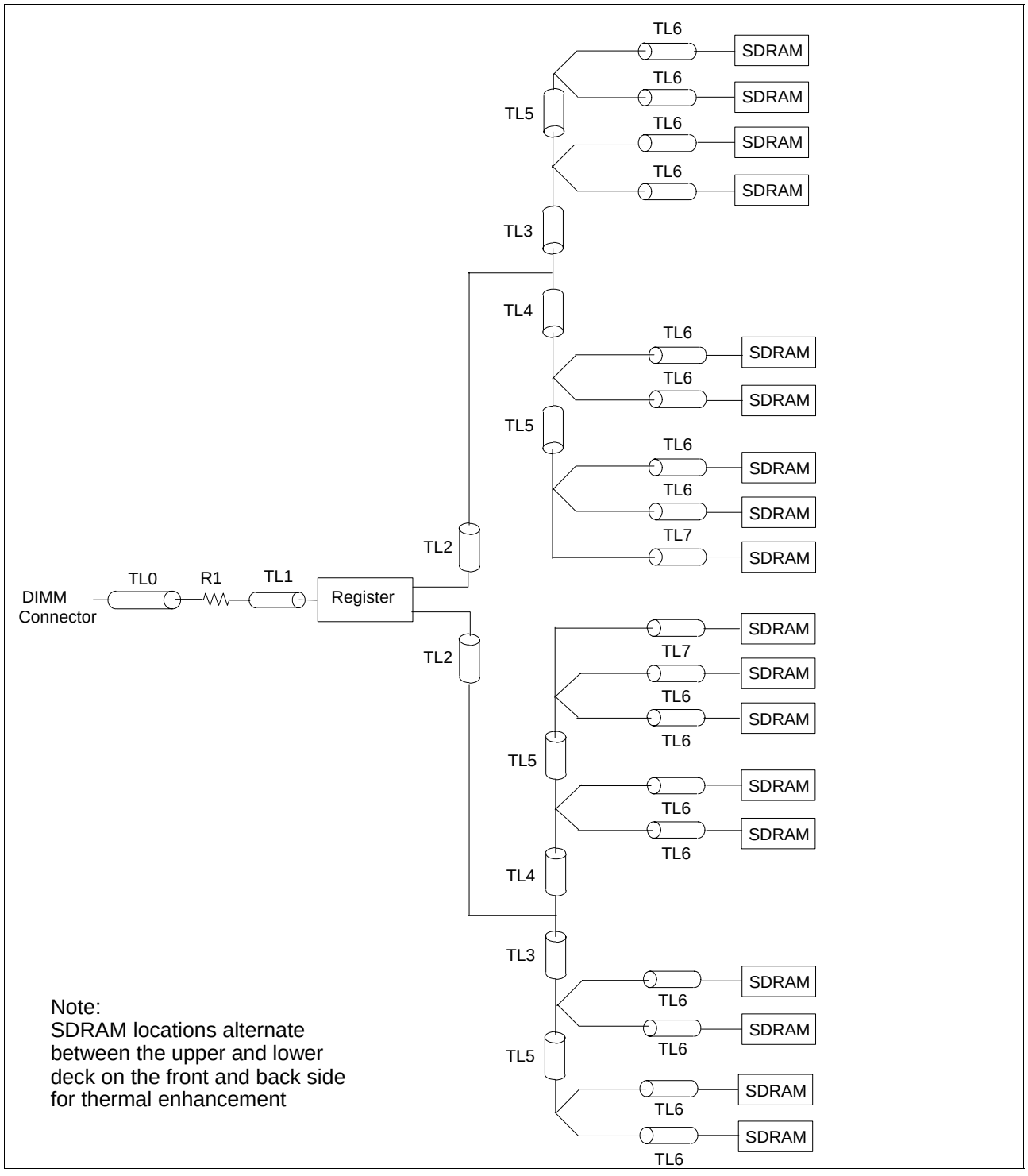
A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C	0.13	0.25	0.56	0.66	0.70	2.81	0.40	0.58	0.07	0.23	0.48	0.61	0.20	0.35	0.49	0.74	22	1
E	0.13	0.23	0.56	0.66	0.70	2.81	0.40	0.58	0.07	0.15	0.48	0.61	0.20	0.35	0.49	0.74	22	1
H	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	22	1
K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch.

Net Structure Routing for $\overline{CS}$ and CKE (Raw Cards C, E, H, and K)

$\overline{CS}$[0:1], CKE[0:1]



Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card C, E, H, and K)

$\overline{CS}$[0:1], CKE [0:1]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 (Ohms)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C	0.14	0.19	0.50	0.51	2.14	3.14	0.45	0.61	0.08	0.23	0.42	0.57	0.11	0.45	0.68	0.83	22
E	0.14	0.19	0.50	0.51	2.14	3.14	0.45	0.61	0.08	0.23	0.42	0.57	0.11	0.45	0.68	0.83	22
H	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	22
K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	22

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Cross Section Recommendations

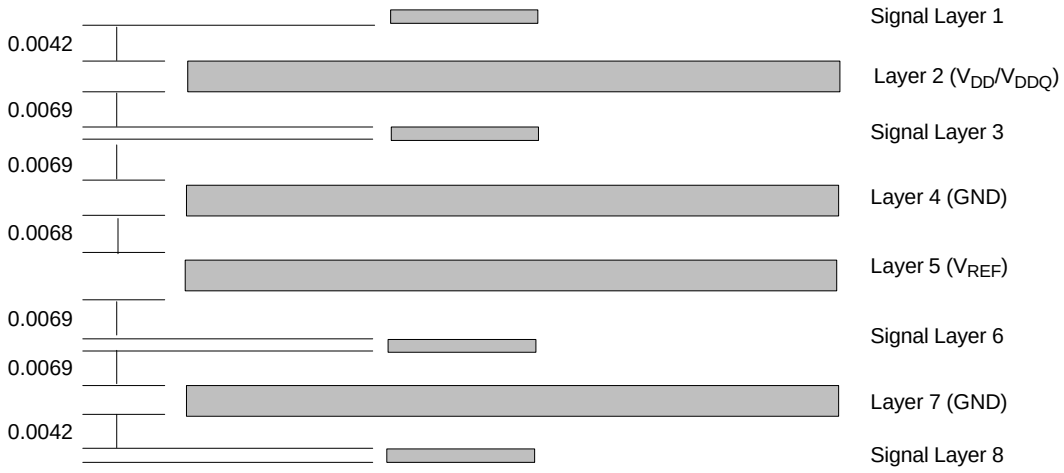
The DIMM printed circuit board design uses eight layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 4 mil wide traces.

Note: The PCB edge connector contacts shall be gold-plated and not chamfered.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	1.6	2.2	ns/ft
Trace velocity: S0 (inner layers)	2.0	2.2	ns/ft
Trace impedance: Z_0 (all layers)	54	66	Ohms

Example Eight Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Impedance Measurement Coupons

In order to allow DIMM manufacturers to verify and monitor the trace impedance (Z_0) listed above, measurement coupons have been added to each of the Registered DIMM designs. There are four single-ended coupons located on each of the four signal layers, as well as a pair of nets wired on the clock signal layer as a differential pair. These nets are all located on the right side of the DIMM.The single ended nets use the EEPROM wires, while the differential pair has been designed in for this purpose. Each net is two inches in length and has a via near a large ground via placed at the bottom of the DIMM. Each net is clearly labeled 1,2,3,4, or DIFF. A Time Domain Reflectometer (T.D.R.) can be used to perform these measurements (for the differential net, odd mode must be used) before DIMM assembly.

Timing Budget

The post-register timings on the Registered DIMMs are critical. The following table describes a preliminary post-register timing budget for a typical DDR PC1600 Registered DIMM. This method is 'Time to Vm' that uses the register timing into its specified test load (instead of t_{CO}, open circuit) and adds or subtracts the timing into the SDRAM net and loads.

DIMM Post-Register Timing

Symbol	Parameter	Time (ns) Set-up	Time (ns) Hold	Notes
t_{CLK}	Clock cycle time	10.0	N/A	1
t_{PD}	Maximum time for the signal to exit the register. This is measured from the rising edge of the register clock input (the falling edge of $\overline{CK}$) to the register output into a standard register test load (30 pF to GND, 50 Ohms to V_{TT}.	-2.8	1.1	1, 2
$t_{NETDELAY}$	Maximum time for the signal to propagate from the register to any SDRAM. The switching point for a rising edge is VREF ± 100mV.	-2.0	0.5	1, 2, 3
t_{REG}	Shift in the register clock in relationship to the SDRAM. The input clocks to the registers and the SDRAM are intended to track, but some error is likely.	–0.10	-0.10	1
t_{IS}	Setup time required for the SDRAM inputs	-1.1	NA	1
t_{IH}	Hold time required for the SDRAM inputs	NA	-1.1	1
t_{Skew*}	Clock jitter and skew on the DIMM	-0.275	-0.2	1, 4
t_{SS}	Simultaneous Switch effect	-0.35	NA	1, 2
t_{XTALK}	Crosstalk Adder	-0.10	NA	
Margin		**3.275**	**0.2**	1

1. The timing values shown are consistent with registers available at the time this specification was written. All registers must meet the combined delay values and ensure positive margin, although the specific delay value for each term may vary.
2. The timing values for tNETDELAY, tPD, and tSS, when added together, define the overall delay from clock at the register to the time when the last re–driven signal arrives at the SDRAM (setup time), or earliest re–driven signal changes state after clock (hold time).
3. The tNETDELAY is determined via simulation analysius. The register driver is simulated into both the standard test load and the actual DIMM net and SRAM loads and the difference is the actual net delay of the DIMM.
4. See the tables below.

*DIMM Clock Contributions (t_{Skew})

t_{Skew} for Setup		Units		t_{Skew} for Hold		Units
DIMM PLL Jitter	0.075	ns		DIMM PLL Skew	0.100	ns
DIMM PLL Skew	0.100	ns		DIMM Clock Net Skew	0.100	ns
DIMM Clock Net Skew	0.100	ns		Total	0.200	ns
Total	0.275	ns				

Serial PD Definition

The Serial Presence Detect function MUST be implemented on the PC DDR SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR SDRAM Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of the SPD data for a PC1600, 512MB (64M X 72), 184 Pin Registered SDRAM DDR DIMM using two physical banks of 32M x 8 DDR200 devices with 13/10/2 addressing and $\overline{CAS}$ latencies of 2 and 2.5.

Serial Presence Detect Example Raw Card Version 'A' (Sheet 1 of 2)

64M x 72 DDR

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total number of bytes in Serial PD Device	256	08	
2	Fundamental Memory Type	SDRAM DDR	07	
3	Number of Row Addresses on Assembly	13	0D	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of Physical Banks on DIMM	2	02	
6 - 7	Data Width of Assembly	x72	4800	
8	Voltage Interface Level of this Assembly	SSTL 2.5V	04	
9	SDRAM Device Cycle Time at Maximum CL (CLX = 2.5)	8.0ns	80	1
10	SDRAM Device Access Time from Clock at CL=2.5	± 0.8ns	80	
11	DIMM Configuration Type	ECC	02	
12	Refresh Rate/Type	7.8µs/SR	82	
13	Primary SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	x8	08	
15	SDRAM Device Attributes: Minimum Clock Delay, Random Column Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	2, 4, 8	0E	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	2, 2.5	0C	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	1	02	
21	SDRAM Module Attributes	Registered with PLL, Differential clock	26	
22	SDRAM Device Attributes: General	V_{DD} ± 0.2V	00	
23	Minimum Clock Cycle at CLX-0.5 (CL = 2)	10.0ns	A0	1
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-0.5 (CL = 2)	± 0.8ns	80	
25	Minimum Clock Cycle Time at CLX-1 (CL = 1.5)	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 1.5)	N/A	00	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on–DIMM pipeline register (that is, Device CL[clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00–FF (Hex).
3. "R" = Alphanumeric revision code, A–Z, 0–9.
4. rr = ASCII coded revision code byte "R".
5. ww = Binary coded decimal week code, 01–52 (Decimal) 01–34 (Hex).
6. yy = Binary coded decimal year code, 00–99 (Decimal) 00–63 (Hex).
7. ss = Serial number data byte, 00–ff (Hex).

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
27	Minimum Row Precharge Time (t_{RP})	20.0ns	50	
28	Minimum Row Active to Row Active Delay (t_{RRD})	15.0ns	3C	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})	20.0ns	50	
30	Minimum Active to Precharge Time (t_{RAS})	50.0ns	32	
31	Module Bank Density	256MB	40	
32	Address and Command Setup Time before Clock	1.1 ns	B0	
33	Address and Command Hold Time after Clock	1.1 ns	B0	
34	Data/Data Mask Input Setup Time before Data Strobe	0.6ns	60	
35	Data/Data Mask Input Hold Time after Data Strobe	0.6ns	60	
36 - 40	Reserved for VCSDRAM	Undefined	00	
41	Minimum Active/Auto–Refresh Time (tRC)	70 ns	86	
42	SDRAM Device Minimum Auto–Refresh to Active/Auto–Refresh Command Period (tRFC)	80 ns	50	
43	SDRAM Device Maximum Cycle Time(tCKmax)	12 ns	30	
44	SDRAM DEvice Maximum DQS–DQ Skew Time (tDQSQ)	0.6 ns	3C	
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	1.0 ns	A0	
46 - 61	Superset information (may be used in future)	Undefined	00	
62	SPD Revision	0	00	
63	Checksum for Bytes 0 - 62	Checksum Data	cc	2
64 - 71	Manufacturers' JEDEC ID Code			
72	Module Manufacturing Location			
73 - 90	Module Part Number			3, 4
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	4
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	5, 6
95 - 98	Module Serial Number	Serial Number	ssssssss	7
99 - 127	Reserved	Undefined	00	
128-255	Open for Customer Use	Undefined	00	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on–DIMM pipeline register (that is, Device CL[clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00–FF (Hex).
3. "R" = Alphanumeric revision code, A–Z, 0–9.
4. rr = ASCII coded revision code byte "R".
5. ww = Binary coded decimal week code, 01–52 (Decimal) 01–34 (Hex).
6. yy = Binary coded decimal year code, 00–99 (Decimal) 00–63 (Hex).
7. ss = Serial number data byte, 00–ff (Hex).

Product Label

The following label should be applied to all DDR-compatible DIMMs, to describe the performance and reference design attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of eight points should be used, and the number can be printed in one, or more, rows on the label. Note that in addition to this label, the manufacturer's name and DIMM assembly part number shall also appear on the DIMM.

Format:

PCwwwwm-aabcd-ef

Where:

wwww: Module Bandwidth
- 1600: 1.6 GB/sec
- 2100: 2.1 GB/sec

m: Module Type
- R = Registered DIMM
- U = Unbuffered DIMM (no registers on DIMM)

aa: SDRAM CAS Latency, with no decimal point (25 = 2.5ns $\overline{\text{CAS}}$ Latency)

b: SDRAM minimum t_{RCD} specification (in clocks)

c: SDRAM minimum t_{RP} specification (in clocks)

d: JEDEC SPD Revision used on this DIMM

e: Gerber file used for this design (if applicable)
- A: Reference design for R/C 'A' is used for this assembly
- B: Reference design for R/C 'B' is used for this assembly
- C: Reference design for R/C 'C' is used for this assembly
- E: Reference design for R/C 'E' is used for this assembly
- F: Reference design for R/C 'F' is used for this assembly
- H: Reference design for R/C 'H' is used for this assembly
- K: Reference design for R/C 'K' is used for this assembly
- Z: None of the 'Reference' designs were used on this assembly

f: Revision number of the reference design used:
- 1: 1st revision (1st release)
- 2: 2nd revision (2nd release)
- 3: 3rd revision (3rd release)
- Blank: Not Applicable (used with 'Z' above)

Example:

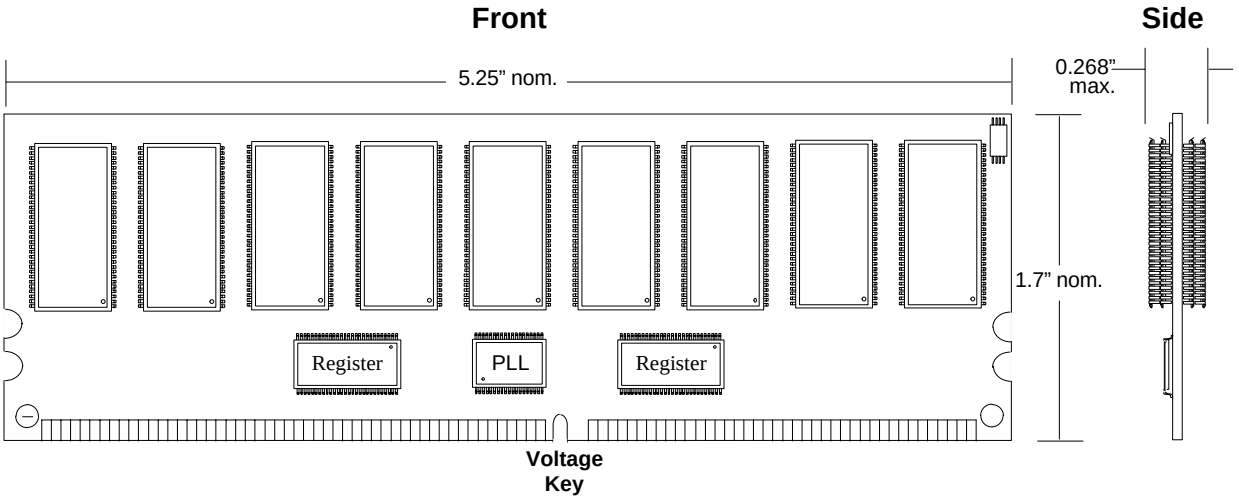
PC1600R-25330-A1
is a PC1600 DDR Registered DIMM
with CL = 2.5, t_{RCD} = 3, t_{RP} = 3
using the latest JEDEC SPD Revision 0.0
and produced based on the 'A' raw card Gerber, 1st release

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 184 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards and Docs.’
3. Scroll down and double click on ‘Publication 95.’
4. Under ‘Outlines/Registrations,’ click on ‘Microelectronics Outlines.’
5. Scroll down and select ‘MO-206’ to download the PDF for this product family.

Simplified Mechanical Drawing with Keying Positions



Note:
The keying in this example defines the DIMM as a 2.5V V_{DD}/V_{DDQ} DDR DIMM.

- The key position defines the voltage for the DIMM: Center = 1.8 Volt V_{DDQ}; Left = 2.5 Volt V_{DDQ}; Right =3.3 Volt V_{DDQ}.

Supporting Hardware

Clock Reference Board

To facilitate the measurement of clock arrival time to the DDR SDRAM for both DDR Unbuffered and Registered SDRAM DIMMs, a ‘Clock Reference Board’ will be released. This board includes the following:

- A frequency synthesizer *to provide 100MHz and 133MHz clocks*
- A clock buffer *to re-drive clocks to the module socket and reference nets*
- A 184P DIMM socket, with three clock inputs wired and *CS and CKE pins tied inactive*
- A ‘Registered’ DIMM reference net *consistent with the JEDEC-approved Registered DIMM Clock Input net structure*
- An ‘Unbuffered’ DIMM reference net *consistent with the JEDEC-approved Unbuffered DIMM clock input structure*
- A clock buffer ‘standard test load’ *to permit characterization of the clock buffer into its test load*

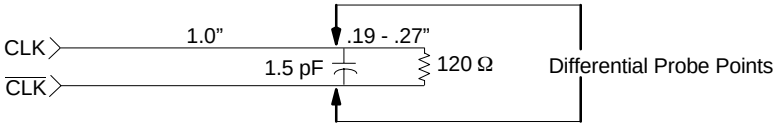
This clock reference board will be made generally available in the industry, and should be used by module producers, as well as system designers, to ensure modules meet the intended clock timings defined in this specification. Every effort will be taken to minimize clock variations and clock skew on these boards.

Application Notes

Clocking Timing Methodology

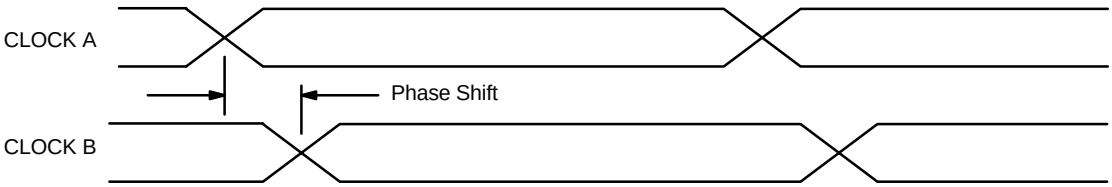
The clock to SDRAM delay is intended to be optimized for high speed operation, while permitting a variety of component layout options. As with Registered DIMMs, the entire clock delay is present between the clock tab pin and the PLL input, and is accomplished via a trace length and a series resistor. This delay should be modeled by the module supplier, to ensure accuracy, if a raw card other than one of the 'reference designs' is utilized. The clock proposed 'Reference Net' below is provided for use during module simulation to ensure an accurate clock delay, since measurement of the delay is impractical (due to the reflections at the clock tab pin).

Registered DIMM Differential Clock Reference Net



Note: Lengths in inches
Z_0 = 60.0 Ohms
t_0 = 2.2 ns/ft

Timing phase shift in two different DDR clock–pair signals is always measured between the two crossing points of the two–clock pairs as follows:



The clock delay from the input of the PLL to the input of any SDRAM is designed to be 0ns (nominal). The clock arrival time at the PLL input should not be adjusted, although sources of timing variation include PLL input capacitance, padding capacitor and termination resistor tolerances, and DIMM impedance variations (the latter items have a minor affect). Due to these variations, it is possible that there will be a difference between the input of the PLL and the input of the SDRAM. A reasonable target for this variation is ±100ps (mean value).

The most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM. The clock reference board Registered DIMM reference net provides the standard net delay for this measurment. The DIMM suppliers must adjust the value of the PLL feedback capacitor to place the clock arrival at the SDRAM on the DIMM within ±100ps of the clock arrival at the Registered DIMM clock reference net (measured as a 'mean', since the PLL and source jitter makes this measurement difficult). This value is a target for DIMM suppliers and does not include worst case contributions of PLL skew, PLL phase error, feedback capacitor variations, and DIMM variations.

On DDR DIMMs, the clock to the register should be in phase with the SDRAM clock. The target range for variation is ±100ps. The actual delay may vary as a result of the input capacitance of the SDRAMs, the register clock input capacitance, PLL output skew variations of the PCB parasitics, and measurement skew (the later two having secondary effects). In the case when the register clocks arrive prior to the SDRAM input clock, this relationship may be adjusted by increasing the value of the register clock padding capacitor.

All changes defined above require simulation to verify the targeted results. Simulation of the clock nets will allow each DIMM manufacturer to determine the most effective method for achieving a 0ps nominal relationship between the register input clock and the SDRAM input clock. It is critical that this analysis be done in order to maintain the required rise-time characteristics as well as signal integrity at the input of

both the SDRAM and the registers. In cases where the register clock cannot be placed in the ideal timing window, post-register timings will need to be adjusted, by the DIMM producer, to ensure robust module operation. (See Post Register Timing Example in this document for summarized clock contributions to the RDIMM budget.)